REPORT RESUMES

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TEACHING ENGINEERING DESIGN, A STUDY OF JOBSHOP.
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THE USE OF A COMPUTER PROGRAM BY ENGINEERING STUDENTS TO SIMULATE A JOB SHOP THAT MANUFACTURES ELECTRONIC DEVICES HAS INDICATED THAT SIMULATION METHODS OFFER REALISTIC ASSISTANCE IN TEACHING. EACH STUDENT IN THE STUDY SUBMITTED SPECIFICATIONS FOR A CIRCUIT DESIGN AND, FROM THE COMPUTER, RECEIVED PERFORMANCE ASSESSMENTS OF THE CIRCUIT WHICH RESEMBLED THE INFORMATION AVAILABLE FROM THE ACTUAL BUILDING OF A DEVICE. SIMPLE PROCEDURES REQUIRING NO COMPUTER PROGRAM BACKGROUND WERE DEVELOPED FOR THE "HOMEWOOD JOBSHOP" PROGRAM. IN 9 WEEKS, STUDENTS WHO KNEW VERY LITTLE CIRCUITRY WERE ABLE TO SOLVE SUCCESSFULLY PROBLEMS OF SUFFICIENT COMPLEXITY TO CHALLENGE EXPERIENCED DESIGNERS. PSYCHOLOGICAL STUDIES RELATED TO LEARNING WERE CONDUCTED WHILE THIS RESEARCH WAS IN PROGRESS. (JM)

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DEPARTMENT OF

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Teaching Engineering Design

A Study of JOBSHOP

by

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PREFACE

It is hoped that this report will be useful to those who teach undergraduate and graduate engineering courses. Our experience indicates it to be most useful fpr students who have moderate knowledge of dynamic elements, but even beginning students can solve simple problems by using only those elements they wish — resistances and sources, for instance. A major outcome of this research is the refinement and improvement of supporting materials for the program. A person should be able to use this program without instruction, and needs to know nothing about computer programming. He is advised to read carefully the instructions in Section I.B and follow through the example provided there. A limited number of copies of Section I.B are available from the authors, without the remainder of this report.

As there at present does not exist within the government any facility for depositing computer programs stored on magnetic tape, we have not been able to deposit a copy with any public agency. There are plans to establish such a facility in the National Bureau of Standards. When it is possible, we will deposit a copy with the Bureau.

The program is available through the SHARE distribution agency. It may be obtained from the IBM Corporation, Program Information Dept., 112 East Post Road, White Plains, New York; Attention: F. A. Marks, Jr.

Many persons have aided in the preparation of this report. It is a pleasure to acknowledge the help of Helen Wirtz, Doris Stude, and Barbara Bricks who aided in preparing the manuscript, and that of James Smith who prepared the illustrations. The students who participated in the summer session were extremely helpful. — Doris Entwisle, W. H. Huggins, Baltimore, Md.
May , 1965

INTRODUCTION

INTRODUCTION

This report is concerned with the Homewood JOBSHOP program, authored by W. H. Huggins. The program is an elaborate digital-computer simulation of an electronic JOBSHOP.

By submitting specifications for a circuit design, with both the kind of components and their joint configuration defined, an engineer can acquire information from the computer like that available from the actual building of a device. The performance of the device may be assessed in many ways, and permanent records are automatically provided.

Major interest attaches to use of this program as a didactic device, but several other interests are also reflected in this report;

a) The refinement and elaboration of the JOBSHOP program.

b) The preparation of adequate documentation; coding forms, and operating descriptions of the program, so that a novice can use the program effectively.

c) Investigation of psychological problems, where possible, in the areas of programmed learning, concept formation, and word association.

Study of the program as a teaching device, the major research effort, involved several groups of individuals: sophomore students, students who had completed a basic course in Introductory Systems and Design, a group of industrial designers, and other individuals in various phases of engineering training. The educational trials of the program and its capability for design-teaching is reported in Section II. Section I gives the technical background for the program, and the documents that have been prepared to aid in its use. Psychological studies are presented in Section III.

A few comments are in order about the history of the program and the current status of the teaching of engineering design before proceeding to Section I, a description of the program as it now exists.

History of Program. A standard course in the curriculum of electrical engineering is "circuit theory." This course is ordinarily given to electrical engineering undergraduates as the first course in engineering *per se* and requires mathematics through the calculus. In the fall of 1961 this course at the Johns Hopkins University was re-named "Introductory Systems and Design" and its content was enlarged to include principles of design (synthesis) as well as analysis. It is difficult to invent exercizes in design, especially with beginning students whose background is as yet limited. To provide opportunities to design while simultaneously avoiding saddling the student with heavy computation or with theory he was unequipped to handle, the first JOBSHOP program was written.[1]

The limitations of the early JOBSHOP, coupled with its apparent success, prompted the preparation of a more extensive program, the HOMEWOOD JOBSHOP. This will be described fully in Section I, so only a brief description is given here. The program will handle circuits having up to 20 terminals, including dynamic units, and will provide extensive information on performance characteristics in both numeric and graphic form. ("Homewood" is the name of one of the campuses of the University where all undergraduates are found.) It is limited to linear systems, or such nonlinear systems as can be adequately approximated by linear models.

---

[1] A write-up of this preliminary program, whose authors are R. P. Rich and N. Lakey, appears as Appendix A.

Current Status of Design Teaching. There has been continuing concern on the part of engineering faculties regarding a very real hiatus in the experience of graduating engineers. The undergraduate curriculum consists almost exclusively of exercises in analysis, in the solving of circuits as given, for instance. Yet a practicing engineer is usually confronted with the opposite problem: how to build a device with given performance characteristics. To imply that there is a sharp division between analysis and synthesis distorts the truth, and of course skill in analysis is necessary, if only to evaluate the products synthesized. Nevertheless, although educational theory is still not robust there is one principle that emerges in one situation after another. This is the principle of specificity: direct practice is the preferred method of training when it is possible. If we wish to teach someone to fly an airplane, it is best for him to practice with an airplane rather than some other kind of vehicle or training device. By the same token one can say that unless specific opportunities to design are provided, it is extremely unlikely that design tactics and principles will be learned by engineering students.

As already mentioned, direct experience in design is difficult to arrange for relatively inexperienced persons. Practical design without feedback concerning results is probably worthless. Yet electronic devices are expensive to build and test, particularly in sufficient quantity for a student to practice something many times, and they also cannot be built rapidly enough to provide immediate feedback. For all these reasons, a JOBSHOP simulation suggests itself as being an ideal pedagogic maneuver.

(1) It permits actual practice with definite knowledge of results.

(2) The information about results is quickly available so students can revise and resubmit designs.

(3) Novices whose background is sketchy can lean on the program to bolster their mathematical and computational skills. It is possible to use the program without knowledge either of digital programming or the techniques needed to solve extremely complicated circuits.

(4) Persuasive and realistic data are provided concerning principles students must master. For instance, tolerances are assigned in such a manner that vagaries of selection may result in better-than-anticipated designs, but the possibility of building several units will demonstrate to the student this kind of fallacy. In building units in an actual JOBSHOP, limitations on quantity may obscure or distort important principles.

It is fair to say that little is known concerning design teaching in spite of the attention that has lately been lavished on this topic. Simulation methods offer a realistic solution for many of the problems posed here, and perhaps the only workable solution aside from preceptorship experience. A computer-based teaching exercise is one approach to teaching design that appeared to merit considerable study.

In actual problem-solving efforts, such programs are already used extensively in industry, and so the training received by students using such a program could provide direct as well as indirect or simulated training.

APPENDIX A

A DESCRIPTION OF THE PRELIMINARY JOBSHOP PROGRAM

THE JOHNS HOPKINS UNIVERSITY

ELECTRICAL ENGINEERING CIRCUITS 52.18

CIRCUIT JOBSHOP SIMULATION

by

Dr. R. P. Rich and Mrs. Nancy R. Lakey
University Computing Center

20 February 1962

CIRCUIT JOBSHOP SIMULATION 11/30/61

INTRODUCTION

Consider the following situation. An engineer designs a circuit, sends the circuit diagram to the electronic JOBSHOP together with a job order for 10 units, and then receives from the JOBSHOP cost information and test results. On the basis of this information he may decide that the circuit is ready for production or he may decide to change the design and try again.

The actual maintenance of a real JOBSHOP of the required capacity (especially when the designers are in fact students) would be expensive and time consuming. The present memo describes a way of simulating the JOBSHOP on a digital computer to save cost and time. The simulation is intended to be realistic in the sense that communication between designer and machine closely approximates (at least in substance) communication between designer and shop.

The simulation is capable of handling static direct-current circuits made up of resistors, voltage sources, and current sources, and of providing input and output (G) parameters for the circuit (optional).

The circuit is specified by a parts connection list (Heath-kit style) rather than directly by a circuit diagram. This list includes one line for each component, giving the physical characteristics of the component and the terminals to which it is connected. A final line specifying the location of ground and the number of units to be constructed is also written.

Any tests to be performed are also specified on the appropriate lines.

The simulator then provides the following output

1) statement if the circuit is infeasible,

2) cost per unit, including any tests required,

3) identification of any burned out components for each unit,

4) listing of requested test results for each unit,

5) input, output parameters for the circuit (optional).

SPECIFICATION OF INPUTS

Four different types of lines may occur in the specification

Resistor - Type 1

Voltage source - Type 2

Current source - Type 3

Last card - Type 4

Types 1, 2, and 3 may each contain the following items

1) Type number

2) Component number

3) Initial junction number

4) Terminal junction number

5) Nominal value

6) Power rating

7) Tolerance

8) Resistance test

9) Current test

10) Current test

11) Power test

12) Cost

SPECIFICATIONS FOR DATA CARDS

Types 1, 2 and 3 should be punched as follows

1) Type number	- Column 6	Items 1-4 are integers*
2) Component number	- Columns 8- 9	
3) Initial junction number	- Columns 10-11	
4) Terminal junction number	- Columns 12-13	
5) Nominal value	- Columns 19-28	Items 5-7 are floating point numbers**
6) Power rating	- Columns 29-38	
7) Tolerance	- Columns 39-48	
8) Resistance test	- Column 50	
9) Voltage test	- Column 52	Items 8-12 are integers
10) Current test	- Column 54	
11) Power test	- Column 56	
12) Cost	- Column 58	

*The decimal point is not written.

**The decimal point must be indicated, i.e. the number ten can be written in two ways,

1) 10.

2) 0.1000E+02

These cards must be followed by a Type 4 card, described below.

The type number must be written for each component or the job will be refused.

If no component number is written, then component number zero is assigned. A component number (1, 2,...) should be assigned if the component is to be tested, to permit easy identification of the test results.

The nodes, or junctions, of the network must be numbered (1, 2,...). The same number must not be assigned to two different nodes, but of course the same node designation is used for all the connections to the same bus.

The two node numbers, Items 3 and 4, must be written for each component, or the job will be refused.

The nominal value, Item 5, must be written in the units appropriate to the type--ohms, volts, or amperes respectively. If it is not actually written, the value zero will be assumed. If the value zero is written (or assumed) for a resistor (Type 1) then the component will be replaced by a zero voltage source for technical convenience.

If the power rating, Item 6, is not written then a rating of one watt is assumed.

The tolerance is expressed as a decimal fraction (e.g. 20 percent is written 0.2).

Items 8-12 are each simply an indication of whether the specified test is to be made or not. If the item is left blank the test is not made; if the test is to be made, a one should be written.

LAST LINE

The last line of the specification carries the following items of information

1) Type number
2) Student identification number

3) Junction number of grounded junction

4) Number of units to be built

5) Option

Items 1 and 3 must be written. Any of 2, 4, which are left blank will be assumed to be zero. If the number of units to be built, Item 4, is zero then only cost information will be printed out, and no units will be built. Item 5 should be one if the G parameters are desired. Otherwise Item 5 should be left blank.

The last card - type 4

1) Type number	- Column 6
2) Student identification number	- Columns 8- 9
3) Junction number of grounded junction	- Columns 10-11
4) Number of units to be built	- Columns 12-13
5) Option	- Column 50

Items 1-5 are integers

TREATMENT OF TYPE 1 CARDS DURING INPUT

When a resistor card is read in during the input pass the following actions are taken.

If the nominal value (Item 5) is zero, it is converted to a voltage source (Type 2).

If the tolerance (Item 7) is not written, or is zero, a tolerance of zero is used. Otherwise, the tolerance is set to the nearest value in the sequence.

.001, .005, .01, .05, .10, .20.

If the power rating is zero, set it to 1 watt. Otherwise set it to the nearest value in the sequence

.1, .2, .5, 1.0, 2.0, 5.0, 10.0, 20.0, 50.0, etc.

It the tolerance (as adjusted) is less than 5 percent, the resistance value is unchanged. Otherwise it is set to the nearest value in the appropriate sequence of standard values (see Table). Then the mean conductance is computed as the inverse of this resistance value.

Then the cost is computed and the next component taken.

Table of RETMA Resistance Values

5 Percent	10 Percent	20 Percent
10	10	10
11		
12	12	
13		
15	15	15
16		
18	18	
20		
22	22	22
24		
27	27	
30		
33	33	33
36		
39	39	
43		
47	47	47
51		
56	56	
62		
68	68	68
75		
82	82	
91		
100	100	100

SOLUTION OF LINEAR SYSTEM

Suppose that a network consists of nodes N(I), I = 1, 2,... connected by resistors, pure voltage sources, and pure current sources in any desired fashion. Suppose further that precisely one of the nodes is grounded (set at zero potential). We then want to find the voltage V(I) at the I-th node, I = 1...N.

Evidently we must solve a linear system

1) $$(A(I, J)) \ (V(J)) = (B(I))$$

In order to do this, if the non-singular matrix (A(I, J)) and the vector (B(I)) can be determined, then the solution of (1) can be carried out by an existing routine.

We therefore attempt to find a simple algorithm for the determination of (A(I, J)), (B(I)) from the specifications of the components. We start from the fact that the sum of currents at any node must equal zero.

The basis of the method is to start with none of the components wired in and

$$A(I, J) = B(J) = 0 \text{ for all } I, J.$$

The components are then wired in to the circuit one at a time, the appropriate changes being made in the matrix A and vector B to take account of the restrictions imposed by each component independently. For voltage sources the order of the original system is increased so that the currents may also be determined.

TREATMENT OF CONDUCTANCES - TYPE 1 CARDS

Let G(I, J) be the conductance of any resistor connecting N(I) and N(J), with an assumed direction of current flow from N(I) to N(J).

Then the current into the I-th node due to this resistor is

$$-G(I, J)(V(J)-V(I)) = -G(I, J)V(J)+G(I, J)V(I)$$

and the current into the J-th node due to the same resistor is the algebraic negative

$$G(I, J)(V(J)-V(I)) = G(I, J)V(J)-G(I, J)V(I).$$

When this resistor is wired into the circuit, therefore, the following changes must be made in (1)

$$A(I, I) = A(I, I)+G(I, J)$$

$$A(I, J) = A(I, J)-G(I, J)$$

$$A(J, J) = A(J, J)+G(I, J)$$

$$A(J, I) = A(J, I)-G(I, J).$$

TREATMENT OF CURRENT SOURCES

Consider any pure current source sending a current C(I, J) from N(I) to N(J). Then the contribution of current into N(I) is -C(I, J) and the contribution of current into N(J) is C(I, J). Since the vector B has been taken over to the right hand side of (1), with change of sign, we must make the following changes in this vector when the current source is wired in

$$B(I) = B(I)+C(I, J)$$

$$B(J) = B(J)-C(I, J).$$

TREATMENT OF VOLTAGE SOURCES

Let E(I, J) be the K-th voltage source to be wired in. This will introduce a new unknown, C(N+K), into the system, namely the current flowing from N(I) to N(J) through the voltage source. But it also introduces a new equation

$$V(J)-V(I) = E(I, J).$$

Hence the system must be expanded from order N+K-1 to order N+K by the following changes

$$A(I, N+K) = A(N+K, I) = -1$$

$$A(J, N+K) = A(N+K, J) = +1$$

$$B(N+K) = E(I, J).$$

OPTION

As an option to the user the program will also find the following parameters,

$$G(1, 1), G(1, 2), G(2, 1), G(2, 2), I1(\text{short}), I2(\text{short})$$

which arise from the two equations,

$$I1 = (G(1, 1))V(1)+(G(1, 2))V(2)+I1(\text{short})$$

$$I2 = (G(2, 1))V(1)+(G(2, 2))V(2)+I2(\text{short})$$

To obtain the desired results, two voltage sources E(3, 1), E(3, 2) are wired into the given system in the following manner:

E(3, 1) is connected between nodes 3 and 1, E(3, 2) is connected between nodes 3 and 2. It is assumed that node 3 is grounded.

This will give two new equations,

$$V(1)-V(3) = E(3, 1)$$

$$V(2)-V(3) = E(3, 2)$$

At this point three linear systems are determined by varying the value of E(3, 1) and E(3, 2).

The first of these systems adds to the existing system the two equations,

$$V(1)-V(3) = 1$$

$$V(2)-V(3) = 0$$

Then the current across E(3, 1) will be G(1, 1) and the current across E(3, 2) will be G(2, 1)

The second system uses E(3, 1) = 0, and E(3, 2) = 1. The respective currents will give G(1, 2) and G(2, 2)

And finally E(3, 1) = 0 = E(3, 2) to determine I1(short) and I2(short).

It should be noted that if the circuit already specifies a voltage source between nodes 3 and 1 or nodes 3 and 2 the linear system is inconsistent and will yield a singular matrix.

TREATMENT OF GROUND

A circuit will not be accepted for analysis unless precisely one terminal, say N(I), is specified as ground. In this case the I-th equation must be replaced by the voltage equation

$$V(I) = 0.$$

If this junction is joined to the network either not at all or by current sources only then on the one hand the remaining voltages are not defined and on the other there would be a net flow of current to ground. Hence before the substitution is made, the program checks to see that at least one of A(I, J) is non-zero for this value of I.

It is necessary that the specification of ground be treated last, lest the I-th equation be further modified after the replacement is made.

REDUCTION OF INANITIES

Consider the expanded system

2) $$A(I, J))(Z(J)) = (B(I))$$

Which results from taking account of all the components in the fashion described above. Notice that the first N of Z(J) are the unknown voltages V(J) and the remainder are the unknown currents through the voltage sources.

Inspect each row vector of the matrix (A(I, J)). If this is not the zero vector, go on to the next.

If the K-th row vector (A(K, J))is zero and B(K) is not zero then the K-th node is joined to the mesh by current sources alone, and no solution exists, alarm and throw out.

If the K-th row vector (A(K, J)) and B(K) are both zero then no information is available about the K-th node, probably because it was not in fact wired into the circuit. In this case the corresponding row and column could be eliminated, but it is probably easier to set the node voltage to zero than to juggle the matrix. So in this case A(K, K) is set to 1. Notice, when this happens Z(K) must be a voltage.

Continue so until no row of (A(I, J)) is zero.

Notice that since (A(I, J)) is symmetric there is no need to check independently for null columns.

COST FORMULAS

The following formulas are used to compute the cost of each component. The constants represent the cost of building the circuit.

Resistor

Cost = square root of power / 70(tolerance +.01) +.10

Voltage source and current source

Cost = power / ± 10(tolerance +.01) +K

where K = .20 for a voltage source and

K = 1.00 for a current source.

An additional cost constant of .10 is added to each component cost for each test made for that component. (This constant can be easily changed if desired.)

RESTRICTIONS

The order of the linear system must not exceed 50. Therefore N = number of resistors + the number of current sources + 2 times the number of voltage sources must not exceed 50. However, if the user desires the G parameters then N must not exceed 48.

APPENDIX B

SAMPLE PROBLEM SOLUTION
BY STUDENTS USING
PRELIMINARY JOBSHOP

SUMMARY

RESULTS PREPARED BY A TEAM OF FOUR STUDENTS

E.E. Circuits 52.18 (January, 1962)

JOBSHOP SIMULATION

PROBLEM

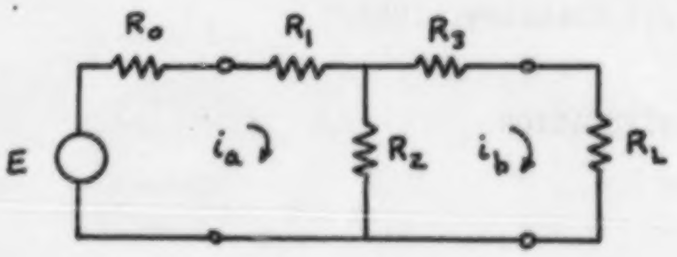
To design an attenuator matched to a 6000 1W. source and to a 5600 ± 10% load. The power delivered to the load must be 0.1 ± 2.5% Watts. The details of the nominal design and the error analysis are given in the later section of this report. Each group member was to submit this design, using one of the four possible combinations of maximum and minimum values for the source and load, to the Circuit JOBSHOP Simulation for construction of ten units. The correct design is as follows: (See figure next page.)

Component	Nominal Value	Spec. Power	Tolerance
E	49.234, 48.746 volts [48.99 ± .5%]	5.0 watts	0%
R_o	600.0	2.0 watts	0%
R_1	327.0 *	1.0 watts	1%
R_2	406.0 *	0.5 watts	.5%
R_3	278.0	0.1 watts	1%
R_L	616, 504 [560 ± 10%]	0.2 watts	0%

*Note: Because I made a calculation error and did not detect it in time to correct the design, the circuits actually submitted to the JOBSHOP used 327.50 and 404.50 for R_1 and R_2 respectively instead of the correct values listed above.

E. E. Circuits

Problem: Design and build the following matched attenuator



$E = 48.99 \pm .5\%$

$R_L = 560 \pm 10\%$

$P_L = .1w \pm 2.5\%$

$R_o = 600 \pm o$

Design

1) Design normalized attenuator with $R_o = R_L = 600$

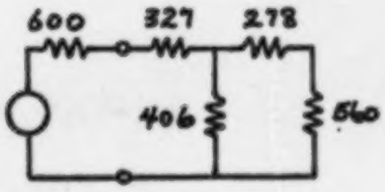
$$A = \frac{V_o}{V_i} = \sqrt{\frac{P_o}{P_i}} = \sqrt{.1} = .316$$

$$R_3 = R_1 = \frac{1-A}{1+A} R_o = \frac{.684}{1.316} .600 = 312\,\Omega$$

$$R_2 = \frac{2^A}{1-A^2} R_o = \frac{.632}{.9} .600 = 421\,\Omega$$

$$R = \begin{array}{c|c|c|l} & a & b \downarrow \times\rho & \\ \hline a & 600 + 733 & -421 & \\ \hline b & -421 & 600 + 733 & \leftarrow \times\rho \end{array} \qquad \rho = \sqrt{\frac{560}{600}}$$

$$R_n^1 = \begin{array}{c|c} a & b \\ \hline 600 + 733 & -406 \\ \hline -406 & 560 + 684 \end{array} \Rightarrow$$



but we used

Nominal Design Values	$R_1 = 327^{\Omega}$	327.5	$E = 48.99^{v}$
	$R_2 = 406^{\Omega}$	404.5	$R_o = 600.0^{\Omega}$
	$R_3 = 278^{\Omega}$	278	$R_L = 560^{\Omega}$

(The values we actually used differed slightly because I made a slide rule error in the first calculation originally.)

Error Analysis by Logarithmic Differentiation:

$$P_L = i_b{}^2 R_L \qquad i_b = \frac{ER_2}{(R_o+R_1+R_2)(R_L+R_2+R_3) - R_3^2}$$

For ease in computation, define $(R_o+R_1+R_2)(R_L+R_2+R_3)-R_3{}^2 \equiv D$

Power

$$P = \frac{E^2 R_2{}^2}{D^2} R_L$$

$$\ln P = 2 \ln E + 2\ln R_2 - 2\ln D + \ln R_2$$

$$\frac{dp}{p} = 2\left(\frac{dE}{E}\right) + 2\left(\frac{dR_2}{R_2}\right) - \frac{2d(D)}{D} + \frac{dR_L}{R_L} \text{ and } \frac{dP}{P} \approx \frac{\Delta P}{P} = \text{fractional change in P}$$

(tolerance)

Evaluate $\frac{d(D)}{D}$

$$\frac{d(D)}{D} = \frac{d(R_oR_2+R_oR_2+R_oR_3+R_1R_L+R_1R_2+R_1R_3+R_2R_L+R_2R_3)}{D}$$

$$= \frac{1}{D}(d\ R_oR_L+R_odR_L+R_odR_2+R_2dR_o+R_odR_3+R_3dR_o$$

$$+R_1dR_L+R_LdR_1+R_1dR_3+R_2dR_1+R_1dR_3$$

$$+R_3dR_1+R_2dR_L+R_LdR_2+R_2dR_3+R_3dR_2)$$

$$= \frac{1}{D}\,[dR_o(R_L+R_2+R_3) + dR_1(R_L+R_2+R_3) + dR_2(R_o+R_1+R_2+R_3)$$

$$+ dR_3(R_o+R_1+R_2) + dR_L(R_o+R_1+R_2)]$$

$$\frac{d(D)}{D} = \frac{dR_o}{R_o}\left(\frac{(R_L+R_2+R_3)R_o}{D}\right) + \frac{dR_1}{R_1}\left(\frac{(R_L+R_2+R_3)R_1}{D}\right)$$

$$+ \frac{dR_2}{R_2}\left(\frac{(R_o+R_1+R_3+R_L)R_2}{D}\right) + \frac{dR_3}{R_3}\left(\frac{(R_o+R_1+R_2)R_3}{D}\right)$$

$$+ \frac{dR_L}{R_L}\left(\frac{(R_o+R_1+R_2)R_L}{D}\right)$$

$$\frac{dP}{P} = 2\left(\frac{dE}{E}\right) + 2\left(\frac{dR_2}{R_2}\right) + \left(\frac{dR_L}{R_L}\right) -2\left(\frac{(R_L+R_2+R_3)R_o}{D}\right)\left(\frac{dR_o}{R_o}\right)$$

$$-2\left(\frac{(R_L+R_2+R_3)R_1}{D}\right)\left(\frac{dR_1}{R_1}\right) -2\left(\frac{(R_o+R_1+R_3+R_L)R_2}{D}\right)\left(\frac{dR_2}{R_2}\right)$$

$$-2\left(\frac{(R_o+R_1+R_2)R_3}{D}\right)\left(\frac{dR_3}{R_3}\right) -2\left(\frac{(R_o+R_1+R_2)(R_L)}{D}\right)\left(\frac{dR_L}{R_L}\right)$$

$$\frac{dP}{P} = 2\left(\frac{dE}{E}\right) -2\left(\frac{(R_L+R_2+R_3)R_o}{D}\right)\left(\frac{dR_o}{R_o}\right) -2\left(\frac{(R_L+R_2+R_3)R_1}{D}\right)\left(\frac{dR_1}{R_1}\right)$$

$$+2\left(1-\frac{(R_o+R_1+R_3+R_L(R_2}{D}\right)\left(\frac{dR_2}{R}\right) -2\left(\frac{(R_o+R_1+R_2)R_3}{D}\right)\left(\frac{dR_3}{R}\right)$$

$$+ \left(1-2\frac{(R_o+R_1+R_2)R_L}{D}\right)\left(\frac{dR_L}{R}\right)$$

Using the following values:

$E = 48.99$ v. ± .5% $\frac{dE}{E} = \pm .5\%$

$R_o = 600\,\Omega \pm 0$ $\frac{dR_o}{R_o} = 0$

$R_1 = 327\,\Omega$

$R_2 = 406\ \Omega$

$R_3 = 278\ \Omega$

$R_L = 560\ \Omega \pm 10\%$ $\qquad \frac{dR_L}{R_L} = \pm 10\%$

$P = 0.1^{w} \pm 2.5\%$ $\qquad \frac{dP}{P} = \pm 2.5\%$

and $D = 1.494 \times 10^6$

The equation becomes:

$$\frac{dP}{P} = 2.5\% = \pm 1\% \pm .547 \frac{dR_1}{R_1} \pm 1.05 \frac{dR_2}{R_2} \pm .496 \frac{dR_3}{R_3}$$

If we specify $\frac{dR_1}{R_1} = \frac{dR_3}{R_3} = 1\%$, and $\frac{dR_2}{R_2} = .5\%$

we obtain:

$$\frac{dP}{P} = \pm 1\% \pm .547\% \pm .502\% \pm .496\% = 2.545\%$$

which is close enough (worst case)

Power analysis

$P = i^2 R$

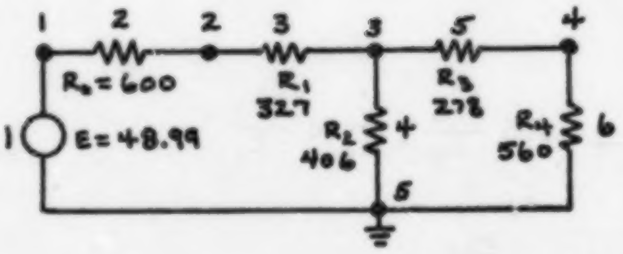
$I\rangle = R^{-1} E\rangle$

$$\begin{array}{|c|}\hline i_a \\ \hline i_b \\ \hline \end{array} = \frac{1}{1.494\text{m}} \begin{array}{|c|c|}\hline 1244 & 406 \\ \hline 406 & 1333 \\ \hline \end{array} \cdot \begin{array}{|c|}\hline 48.99 \\ \hline 0 \\ \hline \end{array} = \overset{I\rangle}{\begin{array}{|c|}\hline 40.75\text{ma} \\ \hline 13.33\text{ma} \\ \hline \end{array}} \begin{array}{c} a \\ b \end{array} \qquad \overset{I^{2}_{,}}{\begin{array}{|c|}\hline 1.665\text{ma} \\ \hline .178\text{ma} \\ \hline \end{array}}$$

$$(i_a - i_b)^2 = (27.42)^2 = .754\text{ma}$$

Component	Nominal Power	Specify Power
E = 48.99 ^{v}	2.0^{W}	5. ^{W}
R_o = 600 Ω	1.0	2.
R_o = 327 Ω	.546	1.
R_2 = 400 Ω	.3065	.5
R_3 = 278 Ω	.0495	.1
R_L = 560 Ω	.09965	.2

Design


1
2
2
3
3
5
4
R_o=600
R_1
327
R_3
278
1
E=48.99
R_2
406
4
R_4
560
6
5

Component	Component Number	Connected to nodes		Nominal value	Power	Tolerance
E	1	5	1	48.99+.5%	5.0	0.0
R_o	2	1	2	600.0	2.0	0.0
R_1	3	2	3	327.0	1.0	0.01
R_2	4	3	5	406.0	0.5	0.005
R_3	5	3	4	278.0	0.1	0.01
R_L	6	4	5	[616, 504]	0.2	0.0

COMMENTS ON THE DESIGN

The nominal design of the circuit was to meet the source and load specifications. The circuit was analyzed to find the nominal powers in the components and, after allowance for power variations with circuit changes, the specified power was set to the next higher value in the given series.

The error analysis used is only an approximate method, and is strictly true only for small changes (small fractional changes) in the elements. In particular, the sensitivity term for changes in the load is zero, that is, the possible 10% variation in the load is not considered at all. This is because the power is maximized for the matched condition, and hence its rate of change with load-value changes is identically zero.

COMMENTS ON THE SIMULATION RESULTS

A large factor in the high cost of some of the units is the necessity of specifying zero tolerance elements for the source and load in order to meet the requirement for specific high or low extreme values. A second factor was the cost of specifying unreasonably high powers [usually about twice the nominal power] so that they would be in the series used in the simulation. The maximum power is delivered to the load when the load is matched to the attenuator. Using only extreme values for the load causes an inherent high degree of mismatch, and so, the power will always be below the matched power. This explains the fact that the power in the load was essentially always below the design specification and seldom above it. As noted before, two of the specified resistance values were in error. These caused the power attenuation to be .0986 instead of the specified .1, resulting in consistently lower powers than would be obtained with the correct circuit. The design was, of course, for the worst case, which would seldom actually occur in practice. All results, therefore, would be expected to be well within specifications if the design and analysis were accurate.

COMMENTS ON INDIVIDUAL RESULTS

Student 1: Used given design with Max. source and load.
Power variation between -.02% and -1.52%.
All units within specifications.
Cost $54.89 each.

Student 2: Used minimum source and load values, given design.
Power variation between -1.95% and -2.69%.
4 units within power specifications.
Cost $54.89 each.

--The power was consistently lower than expected, probably due to the previously explained error in the value of R_2.

Student 3: Used given design, but specified nominal values for the source and load with .5% and 10% tolerances respectively.
Power variation between 0% and -1.91%.
All units within power specifications, but 1 resistor destroyed.
Cost $39.11 each.

--This student asked for extra tests over and above the necessary power test, but they helped to confirm the nominal currents and powers computed for the design. In unit 6, the load resistor was destroyed but should not have been because the .1W power was within the specified .2W. The cost was lower because the tolerances on the voltage source and load were not zero, as they should have been.

Student 4: Used minimum source and load, but did not use given design.

No units within specifications.

Cost $33.55 each.

--He apparently used someone else's design here and did not use the combination of source and load assigned to him. The listing shows an omission in the nominal value of component 20 (source resistance). This was apparently left blank (minus sign 0) in punching the cards. The absence of this 600 load was the main cause of the destruction of the source and 3 attenuator resistors in each unit. The specified power ratings for the components did not allow for the fact that the JOBSHOP would set them to the nearest value in the given power sequence. A power test was not requested for the load, but it was approximately .4 watts.

SUGGESTIONS

As I assume that this type of problem will be assigned next year, I offer the following suggestions based on my experiences with this problem:

It is difficult to get students to work together in a group the way a team of engineers would--they don't always know each other, and can't conveniently get together to hash out a problem. The usual result is that one person ends up doing the work for the others, who don't understand the problem or are too lazy to do their own work. All the work, and the responsibility, lands on one person. The others learn nothing.

This worst case design procedure is good practice but, as you showed in your lectures, hardly a realistic representation of the type of problem an engineer will actually encounter. This could easily be made more realistic by changing the specifications to such as the following: Each student is to individually design 10 units for the specified source and load tolerance. He should try to build them for the least cost per acceptable unit. You might even enhance this by allowing some reject of salvage value for the units that are below specs but have no components destroyed.

Overall, I think that this problem was very good experience and that most students learned a lot from doing it.

SECTION I

Improvement and Thorough Documentation of JOBSHOP

INTRODUCTION AND MINOR PROGRAM MODIFICATIONS

Mention has already been made of the preliminary resistance network program and its replacement by a more elaborate simulation: JOBSHOP. The JOBSHOP program was complete at the start of the present research, but contained a few "bugs" which have subsequently been removed. Its use with several groups of students prompted several things: (A) invention of coding forms that would make the mechanics of using the program as easy and as error-free as possible, (B) a step-by-step description of exactly how one should submit data to the program i.e. how to use the program to "build" and "test" circuits, and (C) a detailed description of the circuit theory, with its underlying mathematics, that makes the simulation possible. In addition, some revisions and additions to the program itself have been made since the start of this research. These will first be described, and then other data related to the program ((A), (B) and (C) above) will be presented.

REVISIONS IN THE PROGRAM

Improved Format of Output Listings. The output formating was extensively revised to provide more explicit headings for various data tables and to assist the user in interpreting the results. For instance, the serial number of each unit of a lot is now printed in one heading of all tables which list D-C operating voltages, system functions, and other test data requested for that unit. Furthermore, legends and headings now accompany all data tables to identify and explain the various types of output data provided. Various diagnostic and warning messages are also printed out when improper circuit connections are specified (for instance, when a voltage source is short-circuited, when the output of an operational amplifier is connected to the input terminal of the circuit, etc.).

Summary Listings for Instructor. The JOBSHOP program remains in the computer while doing successively the jobs specified by any number of students. Provision has been made to produce a complete listing of all input data for use by the supervisor or teacher, and a punched card is produced for each job submitted by every student. These cards contain student identification and other job data, such as serial number, cost of parts, assembly and test costs. These cards may be sorted by student and provide statistical data on usage and expenditures made by the individual students.

Parameter Augmentation Cards. Provisions for randomly perturbing the nominal value of the circuit parameters in accord with their specified tolerances was incorporated in JOBSHOP from the beginning. It soon became apparent, however, that a systematic method for varying the parameter values through a prescribed range would be much more useful for design purposes. Accordingly, provision was made so that any of the parameters may be stepped systematically in small increments through some range of values as successive units in a lot are constructed. In this way, the effect of "worst-case" errors in the components may be measured and used to determine maximum tolerances.

The augmentation card is also useful for changing the connection of any element of the circuit from one unit of the lot to the next. That is, the position in which a component is placed in the circuit configuration may be systematically altered. This powerful feature may be used to study the effect of stray capacitances introduced at different points in the circuit, or to evaluate the contribution of the individual circuit elements to the overall noise-figure of an amplifier.

D-C Operation of Circuit. Since an important part of the design of electronic circuits is concerned with the D-C operating currents and voltages, bias levels, and power dissipation, the program was expanded to incorporate constant voltage sources as one of the kind of element. Data are also provided on the D-C voltage at every node of the circuit and on the D-C current, voltage and power dissipation of each circuit element. By introducing small D-C offset-voltage sources, linear models may be specified that will represent transistors and vacuum tubes quite accurately over a restricted range of operating conditions. (Linear approximation of nonlinear devices.) This feature was used extensively by the students in their amplifier design studies.

Reduction of Round-Off Errors. JOBSHOP first constructs the node-equations for the circuit from the information supplied by the designer (see Section I.C.). This set of node equations is then successively reduced by eliminating the currents and voltages associated with internal nodes until only the input and output nodes remain. The coefficients of this reduced pair of equations are ratios of polynomials in s. In performing the reduction computations, round-off errors often have the effect of adding spurious "stray" capacitances and inductances to the circuit. Of course, stray parasitic effects are also present to some extent in any physical circuit, and one might hope that these round-off errors would add further realism to the simulation. Unfortunately, this is not so because the round-off errors may introduce negative-value effects (thus leading to unrealistic instabilities) and they may be so magnified by the reduction process as to destroy all usefulness of the results.

Considerable effort has been devoted to reducing the effect of these round-off errors. A subroutine was written that automatically transforms the original set of node equations by introducing a new voltage basis for which the inductive and capacitive elements are decoupled insofar as possible. Then at each step in the computation, a "mop-up" subroutine examines the results and decides whether a small non-zero quantity should, in fact, be set to zero. These two subroutines have greatly reduced the effects of round-off errors, but some difficulty still remains, particularly in handling very complicated circuits or where very large and very small values of capacitance occur in the same circuit. A practical solution to these remaining difficulties is to study separately the high- and low-frequency equivalent circuit.

Complete Family of System Functions. Originally JOBSHOP provided only the short-circuit admittances and open-circuit impedence parameters of the two-port equivalent circuit. Other system functions, such as the open-circuit forward and reverse voltage ratios and short-circuit forward and reverse current ratios, are also of interest. Provision has therefore been made for evaluating any member of this entire family of two-port system functions and providing or plotting their values as a function of frequency, or determining their poles and zeros.

Transient Response. Given any system function, it is possible to compute its poles and zeros to gain insight into both the steady-state and transient behavior of the system. The poles and zeros are now available on request.

A program was also written for evaluating and plotting the time-function associated with any system function. Unfortunately, the memory of our IBM 7094 computer does not have room for this last program and it has not been possible to incorporate it in the present version of JOBSHOP. Considerable effort was devoted to rewriting some of the bulkier FORTRAN subroutines in FAP in an attempt to make room, but the complexity of the overall program made this effort unsuccessful.

I.A. REVISIONS IN THE CODING FORM

The first modification was division of the coding form into two separate parts. The first part (on one side of a form) includes the job card, the order card, twenty component cards, and a SNORM card (which can be used as a component card if needed). The second part (on the reverse side of the form) contains four sets of a phasor card, function card, pole and zero card, and blank card package. (The earlier version permitted at most only thirteen components, two phasor and function, and one transient card on one sheet.) The split-form scheme provides for twenty component cards on a sheet and four sets of phasor and function cards on the overleaf. The split-form arrangement is more economical, especially for large jobs. By having the two-part form, coding and key-punching are much easier and less confusing.

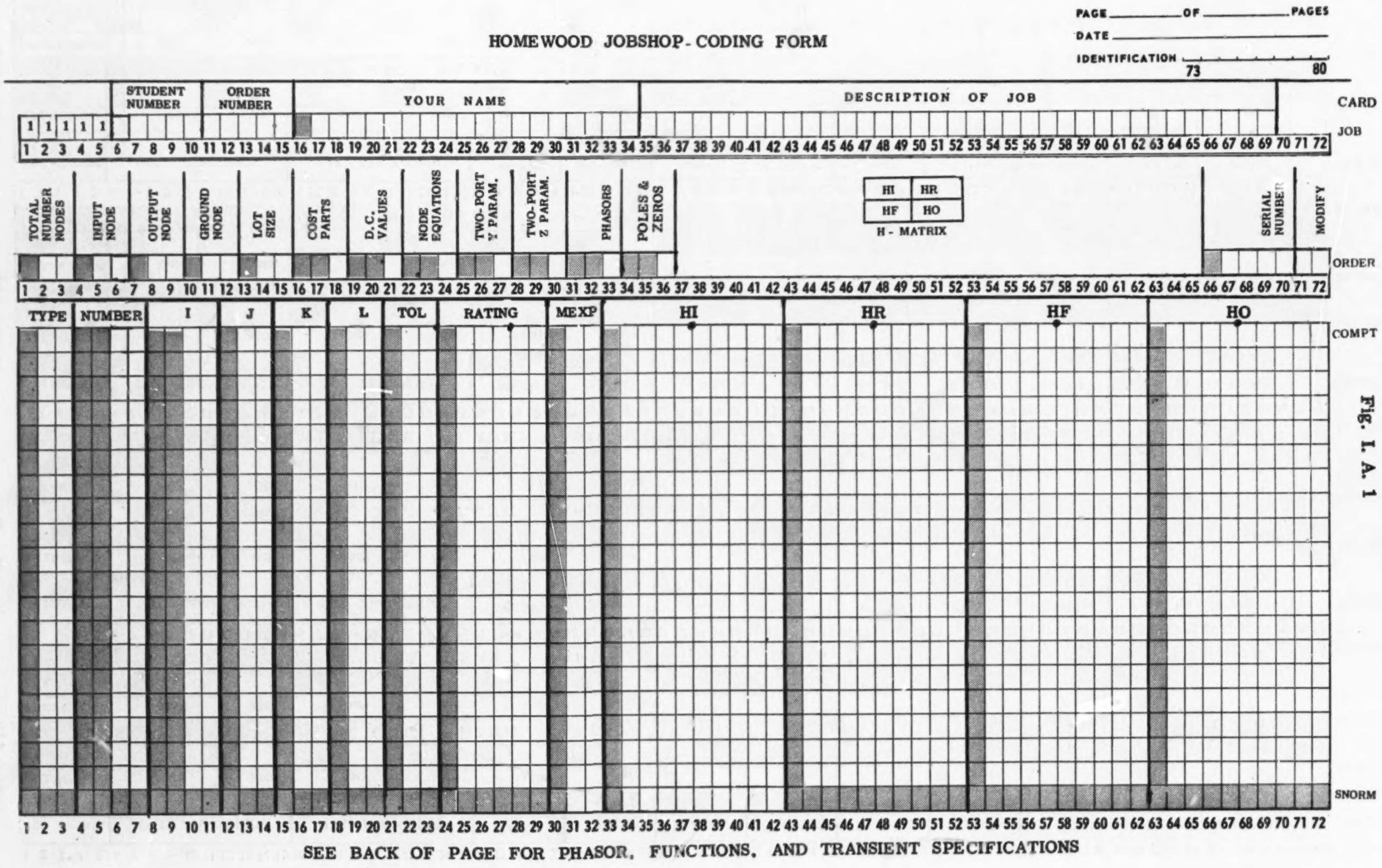
By a major change in the component card the node columns (I, J, K, L) are grouped together. This was indicated because many errors (6.9%) were made when students forgot to label the ground node on a three-terminal device such as vacuum tube. There were also some students who forgot to label the L node on a four-terminal device like a transformer. (Error data supporting these modifications are given in the Error Analysis of Section II.) Also the parameters (HI, HR, HF, HO) appear in adjacent columns. With the parameters grouped in this manner, there is less chance of forgetting to code one of the parameters. Also there was confusion about the fact that the MEXP column affected all the parameters. The grouping of the parameters alleviates this problem.

The new coding form also has the parameters arranged in a new order (HI, HF, HR, HO). This change was made because of the position of the elements in the $\underline{\overline{H}}$ matrix. The natural tendency of a student is apparently to read a matrix by rows, from left to right, starting with the top row of the matrix. Since the parameters used are not always H parameters (e.g. g_m, g_p), a small drawing of the $\underline{\overline{H}}$ matrix on the form has been included to aid the student. With the drawing the student can see the position of an H parameter when a transformation from a $\underline{\overline{G}}$, $\underline{\overline{R}}$, or $\underline{\overline{L}}$ matrix is needed.

The new coding form has on the overleaf four sets of phasor, function, pole-and-zero and blank cards, in that order. This scheme has value because there is no need to rearrange cards after keypunching. The wrong arrangement of the phasor and function cards represented about 3% of total errors made by students, and was particularly troublesome with industrial designers who served as consultants on the project. Also the instruction ONE BLANK CARD printed in the coding area on the correct line reduces the chance of forgetting to insert blank cards.

A reproduction of the revised coding form (two sides) is Fig. I-A-1.

A carefully revised set of directions, with samples, has been prepared to go with the new coding sheet. This forms the next section, I.B.



HOMEWOOD JOBSHOP-CODING FORM

PAGE ________ OF ________ PAGES
DATE ________
IDENTIFICATION ________ 73 80

STUDENT NUMBER	ORDER NUMBER	YOUR NAME	DESCRIPTION OF JOB	CARD
1 1 1 1 1				JOB

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

TOTAL NUMBER NODES	INPUT NODE	OUTPUT NODE	GROUND NODE	LOT SIZE	COST PARTS	D.C. VALUES	NODE EQUATIONS	TWO-PORT Y PARAM.	TWO-PORT Z PARAM.	PHASORS	POLES & ZEROS	SERIAL NUMBER	MODIFY

HI	HR
HF	HO

H - MATRIX

ORDER

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

TYPE	NUMBER	I	J	K	L	TOL	RATING	MEXP	HI	HR	HF	HO

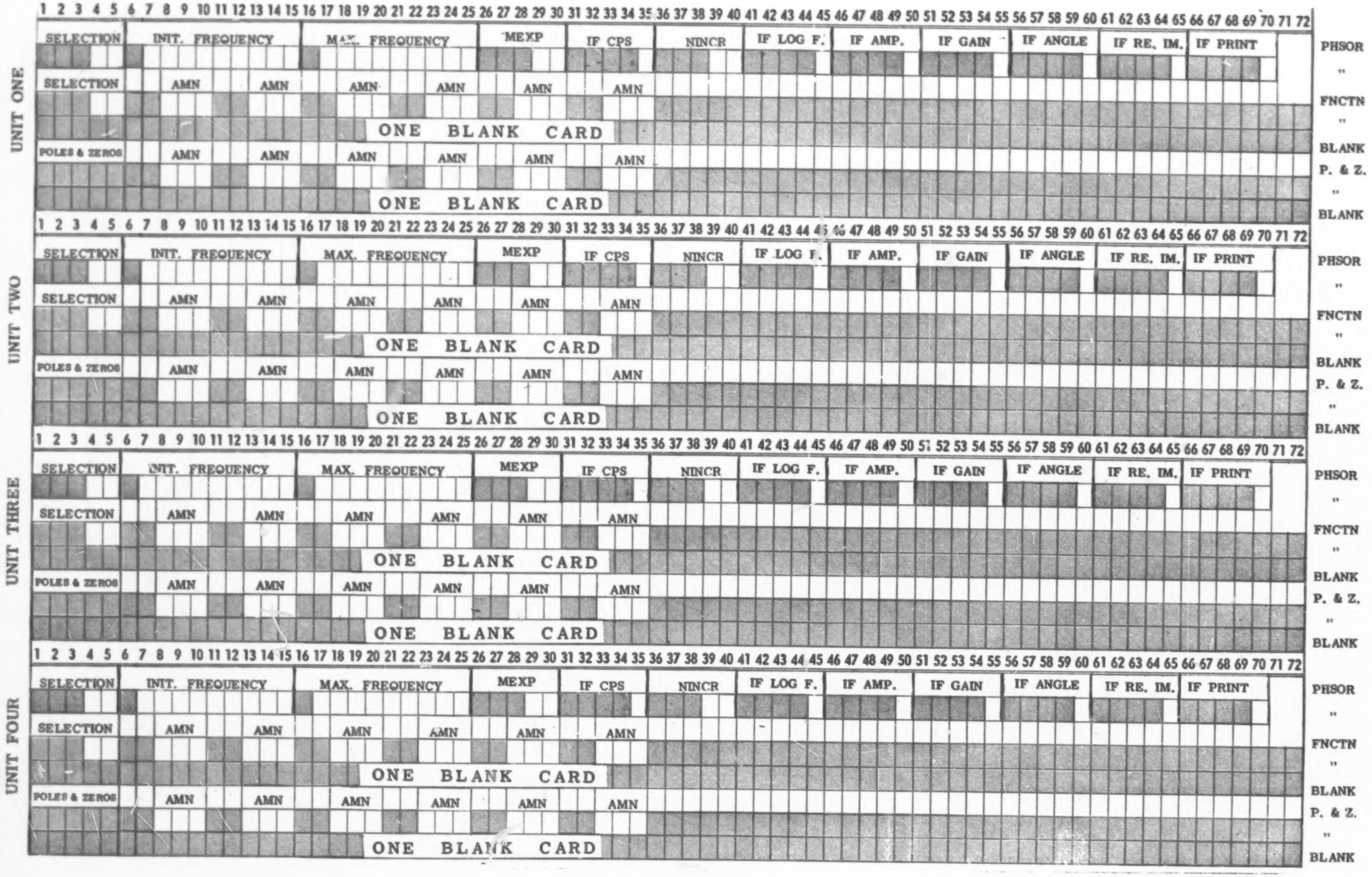
COMPT

SNORM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

SEE BACK OF PAGE FOR PHASOR, FUNCTIONS, AND TRANSIENT SPECIFICATIONS

Fig. I. A. 1


UNIT ONE
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72
SELECTION
INIT. FREQUENCY
MAX. FREQUENCY
MEXP
IF CPS
NINCR
IF LOG F.
IF AMP.
IF GAIN
IF ANGLE
IF RE. IM.
IF PRINT
PHSOR
"
SELECTION
AMN
AMN
AMN
AMN
AMN
AMN
FNCTN
"
ONE BLANK CARD
BLANK
POLES & ZEROS
AMN
AMN
AMN
AMN
AMN
AMN
P. & Z.
"
ONE BLANK CARD
BLANK
UNIT TWO
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72
SELECTION
INIT. FREQUENCY
MAX. FREQUENCY
MEXP
IF CPS
NINCR
IF LOG F.
IF AMP.
IF GAIN
IF ANGLE
IF RE. IM.
IF PRINT
PHSOR
"
SELECTION
AMN
AMN
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AMN
AMN
AMN
FNCTN
"
ONE BLANK CARD
BLANK
POLES & ZEROS
AMN
AMN
AMN
AMN
AMN
AMN
P. & Z.
"
ONE BLANK CARD
BLANK
UNIT THREE
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72
SELECTION
INIT. FREQUENCY
MAX. FREQUENCY
MEXP
IF CPS
NINCR
IF LOG F.
IF AMP.
IF GAIN
IF ANGLE
IF RE. IM.
IF PRINT
PHSOR
"
SELECTION
AMN
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FNCTN
"
ONE BLANK CARD
BLANK
POLES & ZEROS
AMN
AMN
AMN
AMN
AMN
AMN
P. & Z.
"
ONE BLANK CARD
BLANK
UNIT FOUR
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72
SELECTION
INIT. FREQUENCY
MAX. FREQUENCY
MEXP
IF CPS
NINCR
IF LOG F.
IF AMP.
IF GAIN
IF ANGLE
IF RE. IM.
IF PRINT
PHSOR
"
SELECTION
AMN
AMN
AMN
AMN
AMN
AMN
FNCTN
"
ONE BLANK CARD
BLANK
POLES & ZEROS
AMN
AMN
AMN
AMN
AMN
AMN
P. & Z.
"
ONE BLANK CARD
BLANK

SECTION I.B

DIRECTIONS FOR USING THE HOMEWOOD ELECTRONIC JOBSHOP PROGRAM

by HUGH LYNCH

SECTION I.B.

DIRECTIONS FOR USING HOPKINS ELECTRONIC JOBSHOP PROGRAM

Purpose. This document describes the Hopkins Electronic JOBSHOP, how it operates, and how you should submit your orders to have your designs for electronic equipment constructed and tested. In the past, problem assignments were necessarily very narrow in their scope of possible outcomes in order that the teacher could evaluate the work without having to spend an inordinate amount of time in following through the different details. As a result, the student could be given little opportunity for inventing new approaches to the problem or trying alternate schemes.

It would appear that the computer, by actually solving the equations that would otherwise have to be worked out by the designer, is ideally suited for carrying through the consequences of a given design. Then by using these equations, the computer can present the results of any tests or measurements that a technician might make on the actual system. It can introduce random errors into the parameters of the various components in accord with prescribed tolerances, and can assign charges in accord with the cost of the parts that are specified, the measurements that are to be made, and the modifications that are required in the units to make them meet specifications. In other words, by using a computer to simulate an electronic JOBSHOP, we may

1) give the student the opportunity to practice creative design by evaluating the performance of the system he proposes, and
2) introduce economic considerations that have been missing in the past.

Methods. The program compiles the circuit equations on a node basis[1] and automatically solves these equations for the two-port admittance and impedance parameters, which are then used to calculate frequency responses, as well as poles and zeros, of various system functions on request. Provision is made for using as system elements ordinary two-terminal elements - resistors, inductors, and capacitors, as well as unistors. In addition, three and four-terminal (two-port) R, L, and C elements can be entered by specifying the two-port parameters. Thus, provided they are accurately described by their two-port conductance, resistance, or hybrid parameters (and possibly current or voltage offset generators) vacuum tubes and transistors may be used. Two-winding transformers are available as inductance two-ports (four-terminal devices) by specifying the two-port parameters. Provision is also made for incorporating into the circuit ideal operational amplifiers (integrators, scalors, and differentiators), step- and impulse-current sources, and ideal voltage sources.

Usage. How to submit a problem to JOBSHOP.

After designing his system, the user numbers the nodes consecutively beginning with 1, but not exceeding 20. Thus a circuit having a total of 4 nodes, including the datum node, must have the node numbers 1, 2, 3, and 4. The program does not accept other numberings such as 1, 2, 4, 5. Nodes between which large admittances are connected should be assigned node numbers differing by as little as possible. The input, output, and ground terminals are designated by the node numbers assigned respectively to them. The connection of each element into the system is likewise indicated by specifying the numbers assigned to the nodes to which it is attached. In addition, the parameter values, tolerance, and rating of each component is specified.

---

[1] See Section I.C.

Frequency response data may be requested on each unit constructed, the results may be tabulated in numerical form or plotted graphically, whichever is desired. In addition, the program will print out the pole and zero locations of various system functions on request.

The user specifies all work to be done by the JOBSHOP on the JOBSHOP coding form (see attached copy).[2] This coding form has space provided for the several different types of punched cards that are used to enter the job into the computer. Each type of card is discussed individually in the following sections.

1. WORK TITLE CARD

A work title card is required with each new design. A student may enter several new designs at once; these should be grouped together to simplify billing. The work title card contains the following items:

11111	Five ones in columns 1 through 5 identifies a new design work order. This code must appear on every WORK TITLE card submitted to JOBSHOP.
STUDENT NUMBER	In this space the user enters the number assigned to him by the computing center. This space must not include alphabetic symbols.
ORDER NUMBER	Enter here the number of the job to which this computation is to be charged. This space must not

---

[2] See Fig. I.A.1.

	include alphabetic symbols.
YOUR NAME	Enter your name.
DESCRIPTION OF JOB	This space is provided to help you recognize your job and to help you in sorting when you have more than one job. You may choose to use such descriptions as: "Triode Audio Amplifier" or "Twin-Tee Frequency Response".

2. WORK-ORDER CARD

This card specifies the detailed nature of the work to be done by JOBSHOP. It contains spaces for 12 numbers which tell the program the size of the circuit to be built, the number of units to be replicated, and what test results are desired. To the left below are written the column headings which appear on the JOBSHOP coding form. In the spaces assigned, enter each (integer) number as far to the right as possible. (Example: Under TOTAL NUMBER NODES, two spaces are reserved. If your circuit has eight nodes, you should enter -(blank)- 8. The program interprets -eight (blank) as the number 80; since 20 is the maximum allowed here, your design would not be processed.)

TOTAL NUMBER NODES	Enter here the total number of nodes in the circuit (including the ground or datum node). (Maximum number is 20)
INPUT NODE	Enter the number assigned to the node to be treated as the input.
OUTPUT NODE	Enter the number assigned to the node designated as

		the output.
GROUND NODE		Enter the number assigned to the ground or datum node.
LOT SIZE		Enter the number of units to be built to the same design. (Individual units of a given lot may, however, differ due to random errors in the parameters specified to within a tolerance.) Design values of particular parameters may also be changed from unit to unit through the use of component-augmentation cards (see 3A below).
COST PARTS		is the sum of charges for parts used in and tests conducted on your circuit according to a schedule stored in the program. You should enter the numeral:
	0	if no cost data are desired,
	1	to have cost data printed, and punched out on cards for a permanent record.
D.C. VALUES		are the constant voltages at each of the nodes (with respect to ground) and the constant currents through each of the components. Thus, D.C. values give the biasing conditions of the circuit. Enter the number:
	0	if no constant values are desired,
	1	to have constant node voltages printed,
	2	to have constant node voltages and component currents printed.
NODE EQUATIONS		The next entry tells the program whether or not you wish to have the node equations presented, and if so,

in what form. If this entry is set to:

0 no node equations are presented,

1 the program prints out the floating admittance matrix of the nodal equations for the specified circuit,

2 the program prints out the floating admittance matrix of the nodal equations and also punches these equations onto a deck of cards. These cards are used when the unit they represent is to be modified (see below). Each of the next 4 (four) items is set to 1 if output is desired, and 0 otherwise:

TWO-PORT Y PARAM.	1	causes the two-port admittance parameters to be computed and printed.
TWO-PORT Z PARAM.	1	causes the two-port impedance parameters to be computed and printed.
PHASORS	1	causes sinusoidal frequency response data to be computed and presented in accordance with instructions entered below (see section 5).
POLES & ZEROS	1	causes the poles and zeros of functions specified in section 8 to be computed and printed.
SERIAL NUMBER		You may enter here any number of four (or fewer) digits as an aid in identifying and filing this job. If you have called for more than one unit to be constructed, the serial number you have entered here

will be assigned to the first unit of the lot. Each succeeding unit of the lot will be assigned the number one higher than its predecessor. This number will be punched into columns 73-77 of each of the cards returned to you if you call for NODE EQUATIONS to be punched.

To modify a unit previously built, enter a 1 under MODIFY (column 72). The card deck for the unit to be modified (previously punched out as described above under NODE EQUATIONS) should immediately follow this work order card. Follow the node equations deck with component cards specifying new (or altered) circuit elements. If in addition the node numbers are to be re-assigned, enter 1 in column 71 along with the 1 already in column 72 under MODIFY. For instructions on re-numbering nodes, see Modification of a Unit.

3. COMPONENT CARD

One component card is used to specify one component. Thus, to enter a circuit consisting of four resistors, two capacitors, a transistor, and a voltage source, a total of eight component cards will be needed. Each component card bears the following information, in order, from left to right:

TYPE	The type of component to be entered is specified by a component code as listed in the following table: code symbols consisting of only one letter must have that letter in the right hand, or second, column.

Code	Component Type
R	Resistance
G	Conductance
C	Capacitance
L	Inductance
H	Hybrid parameters
UN	Unistor*
IM	Impulse current source. (The direction of the current flow is from node I to node J.)
ST	Step current source. (The direction of the current flow is from node I to node J.)
VS	Constant voltage source. (VS is the voltage at node I minus the voltage at node J.)

To designate an operational amplifier with input from node I and output to node J, enter the input-conductance value under HI, the feedback-parameter value under HR, and the initial condition under HO. To specify the type of feedback element to be used with the amplifier, use the following codes under TYPE:

AC	Accumulator (feedback capacitance).
SC	Scalor (feedback conductance).
DF	Differentiator (feedback inverse-inductance).

---

*A unistor connected from node I to node J and having the parameter G entered under HI causes G units of current to leave node I and enter node J for each volt (relative to ground) present at node I regardless of the voltage at node J.

Several inputs may be connected to the same amplifier by specifying amplifiers of the same type from other input nodes to the same output node(J). The type of amplifier and the value of the feedback parameter is established by the first operational amplifier whose output terminal is assigned to node J.

NUMBER	This is an identifying number to help you locate a specific component easily.
I,J,K,L	In these columns, enter the numbers assigned to the nodes to which the component is attached. The program connects any two-terminal device between the nodes designated under I and J. A three-terminal device has its input at node I, its output at node J, and its common terminal connected to node K. Operational amplifiers automatically have their third terminals connected to the datum node. For resistance, conductance, capacitance or inductance (transformers) two-ports, the primary, or input, terminals are I and K; the secondary, or output, terminals are J and L. Right justify all node numbers; that is, single-digit node numbers must be entered in the right hand, or second column. Thus, enter node 5 as (blank) 5, not as 5 (blank), which would be interpreted as 50.
TOL	Under TOL you may specify the tolerance to be assigned the parameter values. The program assigns parameter

values according to a uniform (rectangular) distribution whose center you specify as the parameter value and whose width you specify as TOL.

If TOL is left blank, the JOBSHOP will use the exact parameter values specified under item 7 (below). To specify a 5% tolerance, enter (blank) 5 under TOL. If you enter a 5 in the first column, leaving the second column blank, the parameter will be assigned a 50% tolerance.

RATING

You may specify the rating of the components to be used in the construction of your circuit. The meaning of RATING depends on the component type as shown in the table given here:

TYPE	RATING means
R (resistance)	power dissipation (watts)
G (conductance)	power dissipation (watts)
C (capacitance)	working voltage (volts)
L (inductance)	D.C. current (milliamperes)

RATING is entered as a decimal number. If you do not explicitly write a decimal point, the program will place one immediately before the last (fifth) digit. You may, however, by explicitly writing a decimal point, place it in any one of the five columns. If you do explicitly write a decimal point, put nothing else in the column occupied by the decimal point.

Example: You may specify a one-half watt resistor by

a) entering .5 in any two adjacent columns under RATING, or b) entering 5 in the last (fifth) column under RATING.

Should you enter a 5 in, say, the fourth column (but not preceed it by a decimal point) you will be charged for a 5-watt resistor.

If the RATING column is left blank, your circuit will operate satisfactorily, although the cost of parts charged may be somewhat unrealistic.

MEXP This column is used to enter a power-of-ten multiplier for all parameter values specified on this card. (There is an exception in the case of the H parameters - see below.) The number assigned as MEXP should be right justified; that is, if it is a single-digit number, say 2, it should be written as (blank) 2. Each parameter value entered under HI,HR,HF or HO, this section, will then be multiplied by 10 to the power 2, or 100. Should you enter the number 2 as 2 (blank), each parameter will be multiplied by 10 to the power 20.

If H parameters are specified under TYPE, the function of MEXP is modified as follows:

HI is multiplied by 10 to the power MEXP
HO is divided by 10 to the power MEXP
HR and HF are unchanged.

If this column is left blank, the program uses the multiplier 10 to the power zero, or 1.

To enter, say, a 2000-ohm resistor, you may elect to a) leave MEXP blank and enter 2000. under HI (see below) or b) write 3 under MEXP and enter 2. under HI. Observe that the decimal-point should always be explicitly given and that it occupies one space on the coding form, as does each digit.

The next four spaces are allocated for the specification of parameter values. The columns are headed HI, HR, HF, and HO respectively. On the coding form a chart shows where these parameters appear in the H matrix. You may, however, wish to use conductance G, resistance R, or inductance L (used for specifying transformers) parameters. Which set of parameters you are using has already been entered under TYPE.

Parameters other than H parameters are entered in the same order as are the H parameters. For example, suppose G parameters are to be used and that they are given in the form

G_{11}	G_{12}
G_{21}	G_{22}

Then G_{11} corresponds to GI and is entered under HI

G_{12} corresponds to GR and is entered under HR

G_{21} corresponds to GF and is entered under HF

G_{22} corresponds to GO and is entered under HO

viz.

HI	HR
HF	HO

Each parameter is specified by a nine-digit number. What this number means depends upon the units the user has chosen when formulating his problem. You may reduce the computation time required, while improving the computational accuracy, by choosing units in terms of which your parameters may be represented as numbers of the order of unity. For example, two sets of consistent units which may be used in certain classes of problems are:

Parameter	For audio amplifiers	For high frequencies
resistance	kilohms	kilohms
conductance	millimhos	millimhos
capacitance	microfarads	milli-microfarads
inductance	henries	millihenries
voltage	volts	volts
current	milliamperes	milliamperes
frequency	kilocycles	megacycles
time	milliseconds	microseconds

If you do not explicitly write a decimal point in these spaces, the program will place the decimal point after the fourth digit (blank columns being read as zeros). You may, however, place the decimal point in any one of the nine columns by explicitly writing one in that column. Put nothing else in the column assigned to the decimal point if you do explicitly write one.

Parameter values for two-terminal elements are entered under HI; the next three spaces are left blank.

Example: to specify a 200 ohm resistor, you may write

a) $\boxed{2}\boxed{0}\boxed{0}\boxed{.}$ in any four consecutive columns under HI or

b) write $\boxed{\ }\boxed{2}\boxed{\ }\boxed{\ }\dot{}\boxed{\ }\boxed{\ }\boxed{\ }$ in the second column as shown.

Further examples, illustrating the way a circuit may be submitted to JOBSHOP, show how you may enter vacuum tubes and transistors as circuit elements. They are given at the end of this section.

3a. COMPONENT AUGMENTATION CARD

Provision has been made for modifying the parameters of the components specified in successive units of a lot. This is done by following a component card with an augmentation card. A plus sign (+) in either the first, second, or third column tells the computer that the card is an augmentation card. The remaining numerical fields of the augmentation card are identical to those of the component card. Any values entered in the columns of an augmentation card will be added to the corresponding values of the immediately preceding card before each successive unit of the lot is manufactured. To illustrate, suppose that resistor R_3 is to have the value 8 in the first unit, the value 9 in the second unit, and the value 10 in the third unit manufactured. Assuming that R_3 is connected between nodes 5 and 7, the component card would read

```
R3          5  7                       8.0
```

It would be followed immediately by an augmentation card punched to modify the resistance value by the desired increment, viz.

```
R3          5  7                       8.0
+                                      1.0
```

The augmentation card may be used to change any (or several) numerical values on a component card. For instance, the tolerance may be changed; or the node numbers I, J, K, and L may be altered, thus enabling the designer to move a component around to different places in the system from one unit to the next.

Since an augmentation card modifies the preceding card, it is possible, by following one augmentation card with a second one, to vary the value of the augmentation from one unit to the next. In fact, one may specify any desired sequence of numerical values. For instance, suppose that R_3 is to take on the values 1, 4, 9, 16, 25 in the successive units of a lot of 5. The values to be entered on successive augmentation cards are easily determined by forming successive differences of the sequence of desired values. To produce the sequence given above, form successive differences by making a table as follows:

> In a vertical column, write the sequence of values desired; write the difference between successive pairs of entries in the next column; repeat until the last column is reduced to one entry. Thus:
>
> | | | | | |
> |---|---|---|---|---|
> | 1 | | | | |
> | | 3 | | | |
> | 4 | | 2 | | |
> | | 5 | | 0 | |
> | 9 | | 2 | | 0 |
> | | 7 | | 0 | |
> | 16 | | 2 | | |
> | | 9 | | | |
> | 25 | | | | |
>
> The leading value in successive columns is the value required in the successive augmentation cards. Since the third and higher differences are all zero in this case, only the original parameter card and two augmentation cards are needed to generate this sequence of 5 parameter values.

In the example just given, the parameter value was increased. It is also possible to reduce a parameter value. The code for the augmentation card is still a + in column 1, 2 or 3; however, the numerical value of the augmentation is negative. Thus to reduce the value of capacitor C_2 (connected between nodes 3 and 4) from .1 microfarads to .03 microfarads on the next unit, use the following set of component and augmentation cards:

C_2	3	4	0.1
+			-0.07

4. SNORM CARD

This card must follow immediately after the last component card. It contains the nominal operating frequency magnitude in radians per unit time. The value of SNORM used by the program is the number entered under HI on this card multiplied by 10 to the power MEXP, where MEXP is the number entered under that heading on the SNORM card. The program uses SNORM to rescale the equations, thus reducing roundoff errors. Unless you are interested in the behavior of your system at frequencies very high compared to the unit of frequency selected under item 3., this section (component card), you will probably want to make SNORM = 1.0.

The specification for the SNORM card is the last item on the front of the JOBSHOP coding form. Should you wish to submit to JOBSHOP a circuit design having more circuit elements (20 or more) than there are spaces on the coding form, do not enter the SNORM card after the nineteenth component. Instead, use another coding form to list the rest of your components. Place the SNORM card after the last component card.

Turn to the reverse side of the coding form to specify what output data you desire and the form in which they are to be presented. Note that the form is divided into four identical horizontal strips by lines on which are printed the column numbers (from 1 to 72). Each strip consists of seven lines which may be used to enter three different types of cards. A description of the specification and purpose of each of these card types follows.

5. PHASOR CARD

If you desire steady-state frequency response characteristics of your design, you will have already entered a 1 under PHASORS (column 33) on your WORK ORDER CARD. The PHASOR CARD and a corresponding FUNCTION CARD are used to describe what frequency data you require and how it is to be presented. The items to be entered on this card are described in the following section, beginning with the first item on the left of the coding form.

SELECTION	Since two cards, a PHASOR card and a FUNCTION card, are needed to order frequency-response data, it is necessary to provide a way for the program to identify, or associate, the correct FUNCTION card with each PHASOR card. Enter under SELECTION any two-digit number; enter the same selection number on the FUNCTION card corresponding to this PHASOR card. From here on, the PHASOR card and the FUNCTION card bearing the same selection number will be said to be "associated."

INIT. FREQUENCY The number entered here, multiplied by 10 to the power MEXP (columns 29 and 30 - see below), is the initial, or lowest, frequency for which frequency data will be computed. Initial frequency is to be entered as a decimal number. You may enter the desired initial frequency anywhere in the allotted space (columns 7 - 15) provided that you explicitly write the decimal point. Enter nothing else in the block in which you write the decimal point. If you omit the decimal point, the program inserts one after the third digit. Thus, to enter a lowest frequency of 15, you may write "15." in any three consecutive columns, or you may enter "(blank) 15" in the first three columns. The program will interpret the number as 15 radians (or kiloradians or megaradians) per second (or millisecond or microsecond) depending on the system of units you have decided to use (see above Section 3 - COMPONENT CARD). You may elect to have the frequency expressed in cycles, instead of radians; enter the number 1 under IF CPS (column 35). If column 35 is left blank or contains a zero, computations will be made in radian frequency. CAUTION: Do not use zero for initial frequency if you call for frequency data to be plotted on a logarithmic scale (see below - IF LOG F.)

MAX. FREQUENCY The number entered here, multiplied by 10 to the power MEXP (see below) is the highest frequency for which frequency response will be computed. It is entered in

	exactly the same way as was INIT. FREQUENCY.
MEXP	The number here is a power-of-ten multiplier for INIT. FREQUENCY & MAX. FREQUENCY. If MEXP is entered as "(blank) 2," the numbers entered under INIT. FREQUENCY and MAX. FREQUENCY will be multiplied by $10^2 = 100$. If MEXP is written as "2 (blank)" the highest and lowest frequencies will be multiplied by ten to the power twenty. If MEXP is left blank, the program will use MEXP = 10^0, thus leaving INIT. FREQUENCY and MAX. FREQUENCY unchanged at the values you have written in those spaces.
IF CPS	Enter a 1 here if you wish frequency response data in terms of cycles (kilocycles, megacycles) per unit time. Leave this space (column 35) blank or enter a zero if you wish frequency response in terms of radian frequency.
NINCR	The number entered here is one less than the number of points at which frequency response data are to be computed. If NINCR is left blank (or entered as zero), the program computes frequency response at INIT FREQUENCY only. If NINCR is set equal to 2, phasors are computed at INIT. FREQUENCY, MAX. FREQUENCY, and one intermediate frequency. NINCR may not exceed 50. NINCR must be right justified; that is, if you wish to set NINCR equal to four, you must enter "(blank) 4;" "4 (blank)" will be interpreted as 40. Should you require more than 50

	increments in your frequency response, use several PHASOR cards with INIT. FREQUENCY of the second equal to MAX. FREQUENCY of the first PHASOR card, etc.
IF LOG F.	Enter a 1 here if logarithmic frequency increments are to be used. Enter a zero (or leave blank) if a linear frequency scale is desired. CAUTION: Do not attempt to use logarithmic increments if INIT. FREQUENCY is zero.
	The next five entries are 1 if output is desired for the functions listed on the associated FUNCTION card. If any of these spaces is left blank (or a zero is entered) the output corresponding to that entry will not be computed.
IF AMP	Enter a 1 here if you wish plots of the magnitudes and phase angles of the functions listed on the associated FUNCTION card.
IF GAIN	Enter 1 if you wish plots of the magnitudes in decibels and phase angle (as functions of frequency) of the functions listed on the associated FUNCTION card.
IF ANGLE	If left blank, the angle is plotted on a scale that runs from -200 to +200 degrees. If a 1 is entered, the scale is automatically adjusted to just contain the maximum and minimum angles. If a 2 is entered, the scale runs from -100 to +100 degrees.
IF RE. IM.	Enter a 1 if you wish plots of the real and imaginary parts of the functions listed on the associated FUNCTION card.

IF PRINT — If you require tabulated values of the phasors you have specified, enter a 1 here. The program computes and prints out the magnitude; decibel magnitude; phase angle; and real and imaginary parts of the functions listed on the associated FUNCTION card. CAUTION: when NINCR is a large number and IF PRINT is set equal to one, it is possible to generate a great deal of output. It is usually preferable to ask for tabulated values at only a few frequencies and have the rest of the required points given graphically.

6. FUNCTION CARD

SELECTION — The selection number punched into the FUNCTION card must be the same as the selection number of the PHASOR card with which it is associated. Thus you must enter here the same number that you entered under SELECTION on the PHASOR card specified on the line immediately preceding this one on the coding form. You have specified the type of output desired, the range of frequencies of interest, and the particular phasors to be calculated on that PHASOR card. The FUNCTION card is used to specify the particular functions for which the phasors are to be calculated.

AMN — On the coding form, the FUNCTION card line has six entries labeled AMN. Each of them may be used to enter the three character code for a function whose phasors you wish to have computed. Enter under A one of the letters from the following table.

Z	Open-circuit impedance
Y	Short-circuit admittance
A	Open-circuit voltage ratio
B	Short-circuit current ratio

These Z,Y,A, and/or B functions relate voltages and/or currents between various pairs of terminals (nodes) in the circuit. In particular, the pair of nodes consisting of the input and datum nodes is called the "inport", while the pair consisting of the output and datum nodes will be called the "outport".

Under M, enter the digit 1 if the response is to be measured at the inport, the digit 2 if the response is to be measured at the outport. Under N, enter 1 if the excitation is to be applied at the inport, 2 if the excitation is applied at the outport. The digit 0 may also be entered under N if you have specified an impulse current source on one of your component cards -(Section 3. above.) The response phasor will then be calculated from the pair of terminals between which the impulse source is connected to the inport or outport as specified under M. Transfer functions between various pairs of nodes may be called for: put the impulse source at different locations by using augmentation cards (Section 3-A above).

Examples: B21 is the ratio of output current to input current with the outport short-circuited.

Y12 is the ratio of input current to output voltage with the inport short-circuited.

You may specify as many as six different functions on one FUNCTION card. The same set of phasors, as described on the associated PHASOR card, will be computed and presented for each of these functions.

It may happen that you require different phasors for different functions. If so, you must use two pairs of PHASOR and FUNCTION cards. For example, suppose that you would like to have a logarithmic plot of the voltage ratio A21 between the frequencies 10 cycles per second and 100 kilocycles per second, but require the output impedance Z22 only at the frequencies 100 cycles, 1000 cycles, and 10,000 cycles per second. You could elect to use one pair of PHASOR-FUNCTION cards for the logarithmic plot and another pair for tabulated values of the output impedance. In this case, follow the first PHASOR-FUNCTION pair with a second bearing a different selection number, and omitting the blank card called for on the coding form. You may use as many pairs of PHASOR and FUNCTION cards as you desire.

7. ONE BLANK CARD

One blank card after the last PHASOR-FUNCTION pair tells the program that all the frequency data for this unit have been completed.

8. POLES & ZEROS

If you have specified, by entering a 1 under POLES & ZEROS (column 36 of the WORK ORDER card) that you wish to have the poles and zeros of some of your network functions as part of your results, use this card to specify which functions you would like to have factored into poles and zeros. You may ask for the poles and zeros of any of the functions (up to a maximum of 6 per unit of the lot) which were listed above in the description of the FUNCTION CARD. If you do not require poles and zeros, as indicated by a blank or a zero in the column 36 of the work order card, skip this card.

9. ONE BLANK CARD

This blank card tells the program that no more poles and zeros are to be computed for this unit. The program proceeds with the construction of the next unit of your lot, up to and including the number entered as LOT SIZE (columns 14 and 15 of the WORK ORDER card). If LOT SIZE is 1, follow this blank card with another blank card. If LOT SIZE is 2 or more, tests must be specified for each unit of the lot by following this card with additional pairs of PHASOR and FUNCTION cards and POLE and ZERO cards grouped together for each unit as indicated on the coding form. LOT SIZE is restricted to 10 or less; if more spaces are required than the four provided on the coding form, use the reverse side of another coding sheet.

10. ONE MORE BLANK CARD

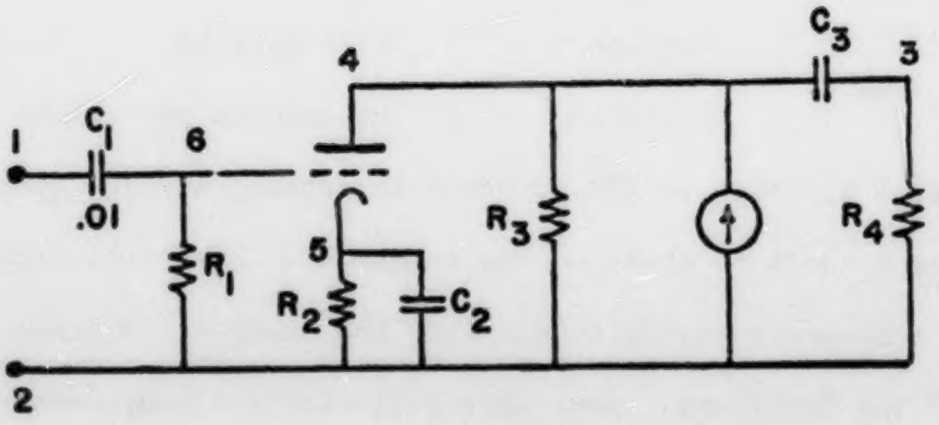
After the last unit of the lot, place one more blank card (i.e. two in a row after the last **POLE & ZERO** card) to prevent destructive readout of the next JOB card. Two blank cards are necessary to signify the end of a job.

Illustration of the Use of JOBSHOP. To illustrate the procedure for submitting a design to JOBSHOP, consider a single-stage triode amplifier using a type 6C5 tube, as shown schematically in figure I.B.1. The vacuum tube is presented by its linearized model with transconductance 2000 micromhos and plate resistance 10,000 ohms. The first step in submitting the design to JOBSHOP is to number the circuit nodes. Note that, in this problem, the input, ground, and output nodes have been assigned the node numbers 1, 2, and 3 respectively. (Refer to Figs. I.B.1 and I.B.2.)

Next, prepare the JOBSHOP coding form. The first line of the coding form begins with the five ones (11111) which indicate that this is a JOBSHOP job card. Enter in order your student or employee number, the order number to which the job is to be charged, and a brief description of the job.

The next card is the WORK ORDER card, on which are entered the TOTAL NUMBER OF NODES in the circuit, and the numbers assigned to the INPUT NODE, OUTPUT NODE, and GROUND NODE in that order. For this example, the number entered under LOT SIZE is 3, so that three units of this design will be replicated. DC VALUES and NODE EQUATIONS have both been entered as 2, so that (a) the biasing voltages and currents will be computed, and (b) the nodal equations will be printed out and punched into cards so that the units may be modified. The rest of the entries on this card are all 1, indicating that each of the listed results is a desired output.

The first unit of the lot has been assigned the serial number 1101. The second and third units will be assigned serial numbers 1102 and 1103 respectively.


C3
4
3
1
C1
6
.01
R3
R4
R1
5
R2
C2
2

The next lines on the coding form are for the specification of COMPONENT cards. Before entering the information required on these cards, you will want to choose a system of units, as discussed in Section 3 (above). Those used in this example are:

Conductance	G	millimhos
Resistance	R	kilohms
Capacitance	C	microfarads
Voltage	V	volts
Current	I	milliamperes
Frequency	f	kilocycles per second

Thus, R 1, which is 330,000 ohms is entered as 330. connected between nodes 2 and 6 as shown on the schematic. Zero tolerances have been used on all components merely to simplify the example. Ratings may be assigned in the usual way. Note that following the component card for C 2, there are two augmentation cards, viz.,

```
C 2   2 5              20.
+                     -18.
+                      16.
```

Thus the value of C 2 used in unit number 1101 will be 20 microfarads, while in unit 1102 C 2 will be

$$C\ 2 = 20. - 18. = 2.,$$

and in unit 1103 C 2 will have the value

$$C\ 2 = 20. - 18. + (-18. + 16.) = 0 \text{ microfarads.}$$

The vacuum tube is represented by its G parameters. For the tube chosen, g_m is 2000 micromhos, which is entered into the JOBSHOP as GF = 2. (millimhos); the plate resistance is 10,000 ohms, so that the plate conductance is

100 micromhos, and this parameter is entered as GO = 0.1 (millimhos). The last item on the front of the coding form is the specification for the SNORM card: SNORM has been entered as 1.0.

Reverse Side of the Coding Form. In this example problem, the first PHASOR-FUNCTION card pair has been assigned the selection number 1. The values of the input and output impedances, Z11 and Z22; and the voltage gain A21 are to be tabulated at 100,550, and 1000 cycles per second; in the system of units chosen for this problem, this means that INIT. FREQUENCY is to be entered as .001 and MAX. FREQUENCY as .1 (kilocycles per second). That the frequency is to be expressed in cycles is indicated by the 1 under IF CPS. The number of increments is 2, and since the test frequencies differ by a constant (450 cycles per second), IF LOG F has been left blank so that a linear frequency scale will be used. The 1 entered under IF PRINT means that these data will be presented in tabular form.

For this first unit of the lot, two sets of phasors have been requested, so the blank card (called for after the first PHASOR-FUNCTION card pair) as well as the following POLE and ZERO card, has been omitted. The second PHASOR card, with selection number 2, specifies plots of voltage gain A21 and output impedance Z22 on a logarithmic frequency scale from 1 cycle per second to 10,000 cycles per second. In kilocycles, therefore, INIT. FREQUENCY and MAX. FREQUENCY are .001 and 10. respectively. NINCR has been chosen as 40, giving 10 data points per decade frequency change. Since the voltage gain is most conveniently given in decibels, while the complex impedance is most conveniently given in rectangular form, 1's have been entered under IF GAIN and IF RE IM.

Following the blank card which indicates the end of phasor calculations for this unit is the POLE & ZERO card. Poles and zeros of A21 and Z22 have been requested. A blank card indicates that no more poles and zeros are to be computed for this unit.

For the second unit of the lot, a PHASOR-FUNCTION card pair bearing the selection number 3 calls for a decibel versus logarithmic frequency plot of the voltage gain A21 between 1 cycle per second and 10 kilocycles per second. A blank card indicates that this is the only phasor required on this unit. The POLE and ZERO card calls for factorization of A21 and Z22. A blank card signifies the end of tests on this unit.

The PHASOR card for the third unit of the lot bears the same selection number, 3, as did the previous PHASOR-FUNCTION card pair. Thus the voltage gain A21 will be the only function for which phasors will be computed. The particular phasor required is again a decibel versus logarithmic frequency plot from 1 cycle to 10 kilocycles per second. A blank card signals the end of phasor calculations. Poles and zeros are ordered for A21 and Z22. Then two blank cards indicate the end of computations on this design.

Results. On the print-out which you receive from JOBSHOP program, many of the results are presented in scientific power-of-ten notation. For example, .395636E-03 should be read as $.395636\text{x}10^{-3}$, while -.15915E 02 should be read as $-.15915\text{x}10^{2}$ or -15.915. Similarly, S 3 means s^3, where s is the complex frequency variable.

The first items which you will find on the printout you get back from the JOBSHOP (and on the sample printout reproduced here) are replicas of the JOB card, WORK ORDER card, and all the COMPONENT cards you entered. There follows a list of the parts you have ordered for this design together with their costs. The next entry is a tabulation of the elements of the floating admittance matrix which is the basis of all computations made by the JOBSHOP program. On the reproduced computer printout (pp. 81 -93), have been written the six Kirchoff nodal equations (only five are independent) which describe the system. The coefficients of the various node voltages have been collected together, then written in matrix form, after which a factor 1/s has been removed and numerical values substituted. The row and column in which the matrix element is to be found are listed under L and M respectively, on the print-out. Thus to check the entry in row 2, column 5, we read

```
L    M    INVERSE INDUCTANCE    CONDUCTANCE    CAPACITANCE

2    5          0. S 0          -.5000E 00 S 1  -.2000E 02 S 2
```

which we interpret as 0 - .5s - 20.s^2, or .5 millimhos conductance in parallel with a twenty microfarad capacitor. Any matrix elements which do not appear in this table (e.g. L = 5, M = 3) are zero. The current source appears in row 2 and in row 4; the -1 entered under L indicates that this is a source current, appearing on the right hand side of equations 2 and 4.

The next entry is a table showing the D.C. voltages at each of the nodes in the circuit. It is followed by a table of the voltages across, the current in, and the power dissipated by each of the components. You should check here to see if any of the ratings entered on your component cards has been exceeded. Port 1 of the tube means the pair of nodes specified under I and K (consisting of the grid and the cathode), while port 2 means the pair of nodes specified under J and K (consisting of the plate and the cathode). Thus, the voltage at port 1 means the voltage from the grid to the cathode, while the power at port 2 means the plate dissipation of the tube.

The two-port admittance parameters are given as ratios of polynomials in s. For example, the transfer admittance Y_{21} is

$$Y_{21} = \frac{.128000\text{E }00\text{ S }2 \qquad .512000\text{E }01\text{ S }3}{.395636\text{E}-01\text{ S }0 \qquad .116232\text{E }01\text{ S }1 \qquad .418056\text{E }01\text{ S }2 \qquad .256000\text{E }01\text{ S }3}$$

which means that $Y_{21} = \dfrac{.128s^2 + 5.12\, s^3}{.039 + 1.1625s + 4.18s^2 + 2.56s^3}$

The fact that Y_{12} does not appear in this table signifies that its value is zero.

The two-port impedance parameters are given in exactly the same form as are the two-port admittance parameters.

The next item on the computer print-out is a replica of the first PHASOR-FUNCTION card pair for this unit. There follows a tabulation of the phasors called for by this pair of cards. Then the next PHASOR-FUNCTION card pair is replicated after which the plots called for thereon are printed out. Note that the frequency scale runs vertically beginning with INIT. FREQUENCY at the top. Frequency values are given in scientific power-of-ten notation.

The function named above the plot (in this case AMPLITUDE RESPONSE IN DB of A_{21}) is plotted in asterisks (*). The function named below the plot (in this case PHASE ANGLE IN DEGREES of A_{21}) is plotted in periods (.).

Finally, the POLE and ZERO card specifications are printed out, followed by the poles and zeros of the required functions. Thus, for example,

$$A_{21} = A \frac{s^2 (s - .025)}{(s - .18759)(s - .03884)(s - .303)}$$

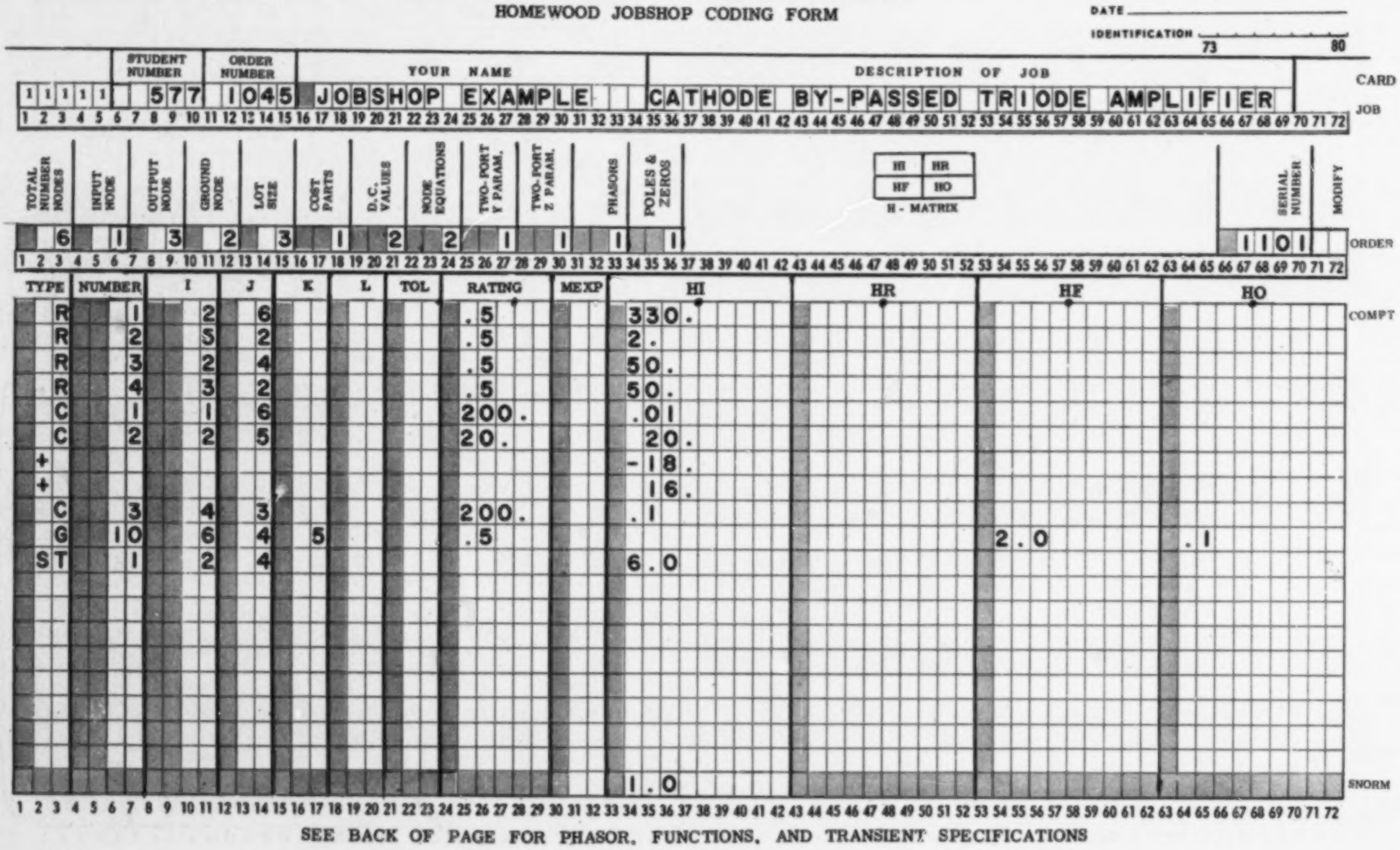
The magnitude A of A_{21} is seen to be the high frequency limit of A_{21} which has been previously calculated to be 14.2.

The print-out for the other two-units is, except for changes in some of the numbers, the same in every respect as this first one.

After all test results for each unit of the lot have been completed, the final item on the JOBSHOP print-out is an invoice, on which are summarized the cost of parts, assembly costs, and the cost of the various tests performed on the units. (It should be pointed out that the costs included in this invoice are not the costs of computing. Computing machine time will be charged to the job number listed on the JOB card (see section 1 above). Charges listed on this invoice comprise part of the simulation which is JOBSHOP.)

Sample JOBSHOP print-out for example of cathode by-pass triode amplifier described in text. For the first unit only, some explanations have been added to the print-out. The print-out for the third unit differs only in numerical details from that for the first two units. Therefore it has not been reproduced here.

FIG. I.B.2. CODING FORM FOR CATHODE BY-PASSED TRIODE AMPLIFIER



HOMEWOOD JOBSHOP CODING FORM

PAGE ________ OF ________ PAGES
DATE ____________________
IDENTIFICATION ____________ 73 80

	STUDENT NUMBER	ORDER NUMBER	YOUR NAME	DESCRIPTION OF JOB	
1 1 1 1 1	577	1045	JOBSHOP EXAMPLE	CATHODE BY-PASSED TRIODE AMPLIFIER	CARD JOB

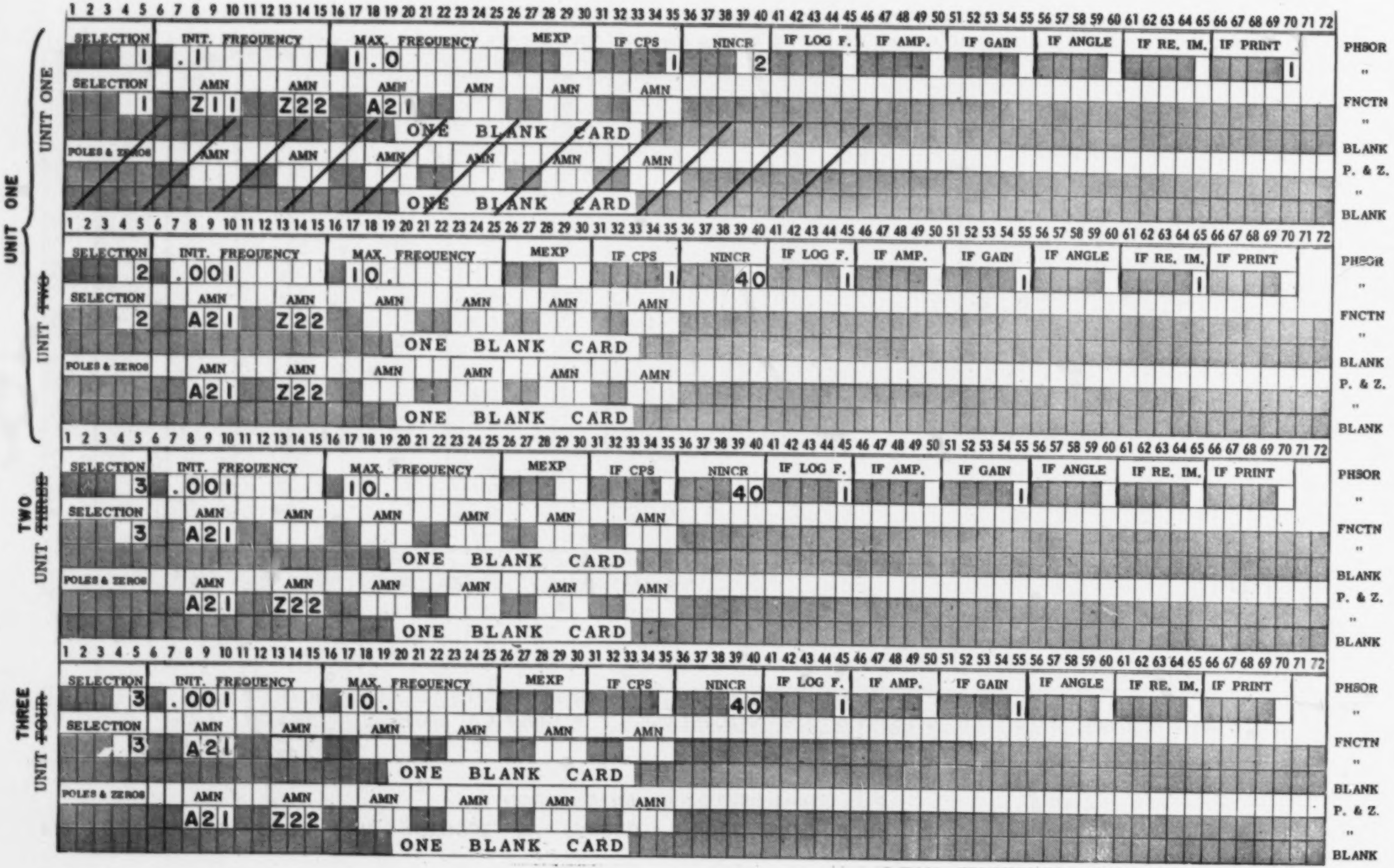
TOTAL NUMBER NODES	INPUT NODE	OUTPUT NODE	GROUND NODE	LOT SIZE	COST PARTS	D.C. VALUES	NODE EQUATIONS	TWO-PORT Y PARAM.	TWO-PORT Z PARAM.	PHASORS	POLES & ZEROS	SERIAL NUMBER	MODIFY	
6	1	3	2	3	1	2	2	1	1	1	1	1101		ORDER

HI	HR
HF	HO

H - MATRIX

TYPE	NUMBER	I	J	K	L	TOL	RATING	MEXP	HI	HR	HF	HO	
R	1	2	6				.5		330.				COMPT
R	2	5	2				.5		2.				
R	3	2	4				.5		50.				
R	4	3	2				.5		50.				
C	1	1	6				200.		.01				
C	2	2	5				20.		20.				
+									-18.				
+									16.				
C	3	4	3				200.		.1				
G	10	6	4	5			.5				2.0	.1	
ST	1	2	4						6.0				
									1.0				SNORM

SEE BACK OF PAGE FOR PHASOR, FUNCTIONS, AND TRANSIENT SPECIFICATIONS



UNIT ONE

UNIT ONE (columns 1–72)

Card	SELECTION	INIT. FREQUENCY	MAX. FREQUENCY	MEXP	IF CPS	NINCR	IF LOG F.	IF AMP.	IF GAIN	IF ANGLE	IF RE. IM.	IF PRINT
PHSOR	1	.1	1.0		1	2						1

Card	SELECTION	AMN	AMN	AMN	AMN	AMN	AMN
FNCTN	1	Z11	Z22	A21			
BLANK	ONE BLANK CARD						
P. & Z. (POLES & ZEROS)							
BLANK	ONE BLANK CARD						

UNIT ~~TWO~~ (columns 1–72)

Card	SELECTION	INIT. FREQUENCY	MAX. FREQUENCY	MEXP	IF CPS	NINCR	IF LOG F.	IF AMP.	IF GAIN	IF ANGLE	IF RE. IM.	IF PRINT
PHSOR	2	.001	10.		1	40	1		1		1	

Card	SELECTION	AMN	AMN	AMN	AMN	AMN	AMN
FNCTN	2	A21	Z22				
BLANK	ONE BLANK CARD						
P. & Z. (POLES & ZEROS)		A21	Z22				
BLANK	ONE BLANK CARD						

UNIT ~~THREE~~ TWO (columns 1–72)

Card	SELECTION	INIT. FREQUENCY	MAX. FREQUENCY	MEXP	IF CPS	NINCR	IF LOG F.	IF AMP.	IF GAIN	IF ANGLE	IF RE. IM.	IF PRINT
PHSOR	3	.001	10.			40	1		1			

Card	SELECTION	AMN	AMN	AMN	AMN	AMN	AMN
FNCTN	3	A21					
BLANK	ONE BLANK CARD						
P. & Z. (POLES & ZEROS)		A21	Z22				
BLANK	ONE BLANK CARD						

UNIT ~~FOUR~~ THREE (columns 1–72)

Card	SELECTION	INIT. FREQUENCY	MAX. FREQUENCY	MEXP	IF CPS	NINCR	IF LOG F.	IF AMP.	IF GAIN	IF ANGLE	IF RE. IM.	IF PRINT
PHSOR	3	.001	10.			40	1		1			

Card	SELECTION	AMN	AMN	AMN	AMN	AMN	AMN
FNCTN	3	A21					
BLANK	ONE BLANK CARD						
P. & Z. (POLES & ZEROS)		A21	Z22				
BLANK	ONE BLANK CARD						

```
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

* * * * * * * * * * * * *  D A T A   I N P U T  * * * * * * * * * * * * * *
----------------------------------------------------------------------------
1111  577 1045 JOBSHOP EXAMPLE   CATHODE BI-PASSED TRIODE AMPLIFIER
----------------------------------------------------------------------------
ND IN OT GD LT  $ DC EC YS ZS FR TR                                  SR MOD
 6  1  3  2  3  1  2  2  1  1  1  1                                  1101 -0
----------------------------------------------------------------------------
TYPE NO  I  J  K  L TOL RTNG EXP    HI         HR          HF          HO
============================================================================
  R   1  2  6 -0 -0  0.  0.50 -0 330.00000  -0.         -0.         -0.
  R   2  5  2 -0 -0  0.  0.50 -0   2.00000  -0.         -0.         -0.
  R   3  2  4 -0 -0  0.  0.50 -0  50.00000  -0.         -0.         -0.
  R   4  3  2 -0 -0  0.  0.50 -0  50.00000  -0.         -0.         -0.
  C   1  1  6 -0 -0  0.200.00 -0   0.01000  -0.         -0.         -0.
  C   2  2  5 -0 -0  0. 20.00 -0  20.00000  -0.         -0.         -0.
  *  -0 -0 -0 -0 -0  0. -0.   -0 -18.00000  -0.         -0.         -0.
  *  -0 -0 -0 -0 -0  0. -0.   -0  16.00000  -0.         -0.         -0.
  C   3  4  3 -0 -0  0.200.00 -0   0.10000  -0.         -0.         -0.
  G  10  6  4  5 -0  0.  0.50 -0  -0.        -0.          2.00000    0.10000
 ST   1  2  4 -0 -0  0. -0.   -0   6.00000  -0.         -0.         -0.
     -0 -0 -0 -0 -0  0. -0.   -0   1.00000  -0.         -0.         -0.


                 COST OF PARTS SPECIFIED ON THIS JOB
      ----------------------------------------------------------
      TYPE     PARTS      NOMINAL    RATING    TOLERANCE     COST
               NUMBER      VALUE
      ==========================================================
        R         1      330.00000     0.500        0.        6.22
        R         2        2.00000     0.500        0.        6.22
        R         3       50.00000     0.500        0.        6.22
        R         4       50.00000     0.500        0.        6.22
        C         1        0.01000   200.000        0.        1.02
        C         2       20.00000    20.000        0.      184.23
        C         3        0.10000   200.000        0.        1.75
        G        10       -0.          0.500        0.       18.00
       ST         1        6.00000    -0.           0.        1.00
      ----------------------------------------------------------
                           COST OF PARTS FOR ONE UNIT IS  $ 230.89


        NODE-PAIR EQUATIONS.  (1/S FACTOR IS REMOVED.  SR 1101)
----------------------------------------------------------------------------
  L  M NA  INVERSE INDUCTANCE    CONDUCTANCE            CAPACITANCE
============================================================================
  1  1  3   0.              S 0   0.             S 1   1.000000E-02 S 2  1
  6  1  3   0.              S 0   0.             S 1  -1.000000E-02 S 2  1
  2  2  3   0.              S 0   0.543030E 00   S 1   0.200000E 02 S 2  1
  3  2  2   0.              S 0  -0.200000E-01   S 1         +            1
  4  2  2   0.              S 0  -0.200000E-01   S 1         +            1
  5  2  3   0.              S 0  -0.500000E 00   S 1  -0.200000E 02 S 2  1
  6  2  2   0.              S 0  -0.303030E-02   S 1         +            1
  2  3  2   0.              S 0  -0.200000E-01   S 1         +            1
  3  3  3   0.              S 0   0.200000E-01   S 1   0.100000E-00 S 2  1
  4  3  3   0.              S 0   0.             S 1  -0.100000E-00 S 2  1
  2  4  2   0.              S 0  -0.200000E-01   S 1         +            1
  3  4  3   0.              S 0   0.             S 1  -0.100000E-00 S 2  1
  4  4  3   0.              S 0   0.120000E-00   S 1   0.100000E-00 S 2  1
```

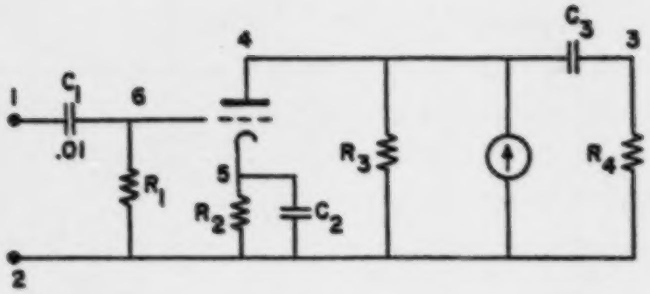


Fig. I. B. 1

The cathode by-pass triode amplifier

$$
\begin{array}{c|c|c|c|}
 & V_g & V_p & V_k \\
\hline
i_g & 0 & 0 & 0 \\
\hline
i_p & g_m & g_p & -g_m-g_p \\
\hline
i_k & -g_m & -g_p & g_m+g_p \\
\hline
\end{array}
$$

at node 1 $\quad C_1S(V_1-V_6) = 0$

" 2 $\quad G_1(V_2-V_6)+(V_2-V_5)(G_2+C_2S)+G_3(V_2-V_4)+G_4(V_2-V_3) = -I_s$

" 3 $\quad C_3S(V_3-V_4)+G_4(V_3-V_2) = 0$

" 4 $\quad G_3(V_4-V_2)+C_3S(V_4-V_3)+g_m(V_6-V_5)+g_p(V_4-V_5) = I_s$

" 5 $\quad (G_2+C_2S)(V_5-V_2)-g_m(V_6-V_5)-g_p(V_4-V_5) = 0$

" 6 $\quad G_1(V_6-V_2)+C_1S(V_6-V_1) = 0$

```
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 5  4  2   0.            S 0   -0.10C0C0E-00 S 1                  +         1
 2  5  3   0.            S 0   -0.50C000E 00 S 1   -0.200000E 02 S 2        1
 4  5  2   0.            S 0   -0.21C000E 01 S 1                  +         1
 5  5  3   C.            S 0    0.26C000E C1 S 1    0.200000E 02 S 2        1
 1  6  3   0.            S 0    G.           S 1   -1.000000E-02 S 2        1
 2  6  2   0.            S 0   -0.303030E-02 S 1                  +         1
 4  6  2   0.            S 0    0.2UC000E C1 S 1                  +         1
 5  6  2   0.            S 0   -0.20C000E 01 S 1                  +         1
 6  6  3   0.            S 0    0.303030E-02 S 1    1.000000E-02 S 2        1
-------------------------------------------------------------------------------
NODE          CURRENT STEP      CURRENT IMPULSE      (EQUIVALENT SOURCES)
===============================================================================
 2 -1  1  -C.60CC00E C1 S 0          +                        +             1
 4 -1  1   0.60CC0CE C1 S 0          +                        +             1

         RESULTS CF DC MEASUREMENTS AT NODES  (SR 1101)
      -------------------------------------------------------------
      NODE NUMBER      VOLTAGE TO GROUND      INDUCTIVE CURRENT
      =============================================================
             1                 0.                  -0.
             2                 0.                  -0.00000
             3                 0.                  -0.
             4               152.94118              0.00000
             5                 5.88235             -0.0000C
             6                 0.                  -0.

        RESULTS OF DC MEASUREMENT OF COMPONENTS  (SR 1101)
      -------------------------------------------------------------
      CMPNT  PORT    VOLTAGE      CURRENT      POWER     RATING
      =============================================================
       G10    1       -5.882       0.          -0.        0.50 POWER
              2      147.059       2.941      432.526
       C 1    1        0.          0.           0.      200.00 VOLTS
       C 2    1       -5.882       0.           0.       20.00 VOLTS
       C 3    1      152.941       0.           0.      200.00 VOLTS
       R 1    1        0.          0.           C.        0.50 POWER
       R 2    1        5.882       2.941       17.301     0.50 POWER
       R 3    1     -152.941      -3.059      467.820     0.50 POWER
       R 4    1        0.          0.           0.        0.50 POWER


              TWC-PORT ADMITTANCE PARAMETERS  (SR 1101)
===============================================================================
CHARACTERISTIC DENOMINATOR POLYNOMIAL IS
  0  0  4   0.395636E-C1 S 0    0.116232E C1 S 1    0.418056E 01 S 2  2
  0  0  4   0.256C00E C1 S 3            +                    +         2

NUMERATOR OF SHORT-CKT CURRENT (DUE TO SCURCES) AT PORT 2 IS
  2 -1  3   0.605C41E C0 S 0    0.665134E 01 S 1    0.153600E 02 S 2  2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y11  IS
  1  1  4   0.395636E-C3 S 1    0.103176E-01 S 2    0.775758E-02 S 3  2
```

MATRIX FORM

	V_1	V_2	V_3	p V_4	k V_5	g V_6
1	C_1S					$-C_1S$
2		$G_1+G_2+G_3$ $+G_4+C_2S$	$-G_4$	$-G_3$	$-G_2-C_2S$	$-G_1$
3		$-G_4$	C_3S+G_4	$-C_3S$		
4		$-G_3$	$-C_3S$	g_p+C_3S $+G_3$	$-g_m-g_p$	g_m
5		C_2S-G_2		$-g_p$	G_2+C_2S $+g_m+g_p$	$-g_m$
6	$-C_1S$	$-G_1$				G_1+C_1S

factor out $\frac{1}{S}$, substitute values

	1	2	3	4	5	6
1	$.01S^2$					$-.01S^2$
2		$.543S$ $+20S^2$	$-.02S$	$-.02S$	$-.5S-20S^2$	$-.00303S$
3		$-.02S$	$.1S^2+.02S$	$-.1S^2$		
4		$-.02S$	$-.1S^2$	$.12S+.1S^2$	$-2.1S$	$2S$
5		$-20S^2-.5S$		$-.1S$	$2.6S+20S^2$	$-2S$
6	$-.01S^2$	$-.00303S$				$.00303S$ $+.01S^2$

```
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NUMERATOR OF SHORT-CKT ADMITTANCE  Y21  IS
  2  1  4   0.128C00E-C0 S 2    0.512000E 01 S 3               +        2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y22  IS
  2  2  4   0.791273E-C3 S 0    0.272027E-C1 S 1    0.189758E-00 S 2  2
  2  2  4   0.358400E-C0 S 3              +                    +        2


                 TWC-PORT IMPECANCE PARAMETERS  (SR 1101)
=====================================================================
CHARACTERISTIC DENOMINATOR PCLYNOMIAL IS
  0  0  5   0.791273E-C5 S 2    0.245915E-03 S 3    0.108606E-02 S 4  3

NUMERATOR OF CPEN-CKT VOLTAGE (DUE TC SOURCES) AT PORT 2 IS
  2 -1  4   C.605C91E-C2 S 2    C.465454E-C1 S 3               +        3

NUMERATOR OF CPEN-CKT IMPEDANCE  Z11  IS
  1  1  5   0.791273E-C3 S 1    0.272027E-01 S 2    0.189758E-00 S 3  3
  1  1  5   C.3584C0E-C0 S 4              +                    +        3

NUMERATOR OF CPEN-CKT IMPEDANCE  Z21  IS
  2  1  5  -0.12800CE-C0 S 3   -0.51200CE 01 S 4               +        3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z22  IS
  2  2  5   0.395636E-C3 S 2    C.103176E-C1 S 3    0.775758E-02 S 4  3


              FRECUENCY RESPONSE CHARACTERISTICS  (SR 1101)
---------------------------------------------------------------------
   L    F-MIN       F-MAX    EXP CPS NINCR LCG  AMPL GAIN ANGL REIM PRNT
=====================================================================
   1   0.100000    1.0CC000 -C    1    2   -0    -C   -0   -0   -0    1
   1  Z11  Z22  A21    -0    -C    -0

FUNCTION    VALUE AT    C.628319E 00 RPS    CR    1.000000E-01 CPS
  Z11       ( 0.33000E 03) + J(-0.15915E C3)  =  ( 0.36637E 03)/ -25.75 DEG          51.28 DB.
  Z22       ( 0.1C568E C2) + J(-0.11524E C2)  =  ( 0.15636E 02)/ -47.48 DEG          23.88 DB.
  A21       (-0.89144E C1) + J(-0.84979E C1)  =  ( 0.12316E 02)/-136.37 DEG          21.81 DB.

FUNCTION    VALUE AT    C.345575E 01 RPS    CR    0.550000E 00 CPS
  Z11       ( 0.33C00E C3) + J(-0.28937E C2)  =  ( 0.33127E 03)/  -5.01 DEG          50.40 DB.
  Z22       ( 0.72658E C1) + J(-0.22744E 01)  =  ( 0.76135E 01)/ -17.38 DEG          17.63 DB.
  A21       (-0.14C59E C2) + J(-0.20630E 01)  =  ( 0.1421CE 02)/-171.65 DEG          23.05 DB.

FUNCTION    VALUE AT    C.628319E 01 RPS    CR    1.000000E 00 CPS
  Z11       ( 0.33C00E C3) + J(-0.15915E C2)  =  ( 0.33038E 03)/  -2.76 DEG          50.38 DB.
  Z22       ( 0.71801E C1) + J(-0.12535E 01)  =  ( 0.72887E 01)/  -9.90 DEG          17.25 DB.
  A21       (-0.14217E C2) + J(-0.11432E C1)  =  ( 0.14263E 02)/-175.40 DEG          23.08 DB.
```

$$Z_{22} = \frac{.395 \times 10^{-3} S^2 + .103 \times 10^{-1} S^3 + .776 \times 10^{-2} S^4}{.79 \times 10^{-5} S^2 + .246 \times 10^{-3} S^3 + .108 \times 10^{-2} S^4}$$

$$= \frac{.776\, S^2 + 1.03\, S + .0395}{.108\, S^2 + .025\, S + .00079}$$

$$\approx \frac{(S + .04)(S + 1.29)}{(S + .188)(S + .04)}$$

```
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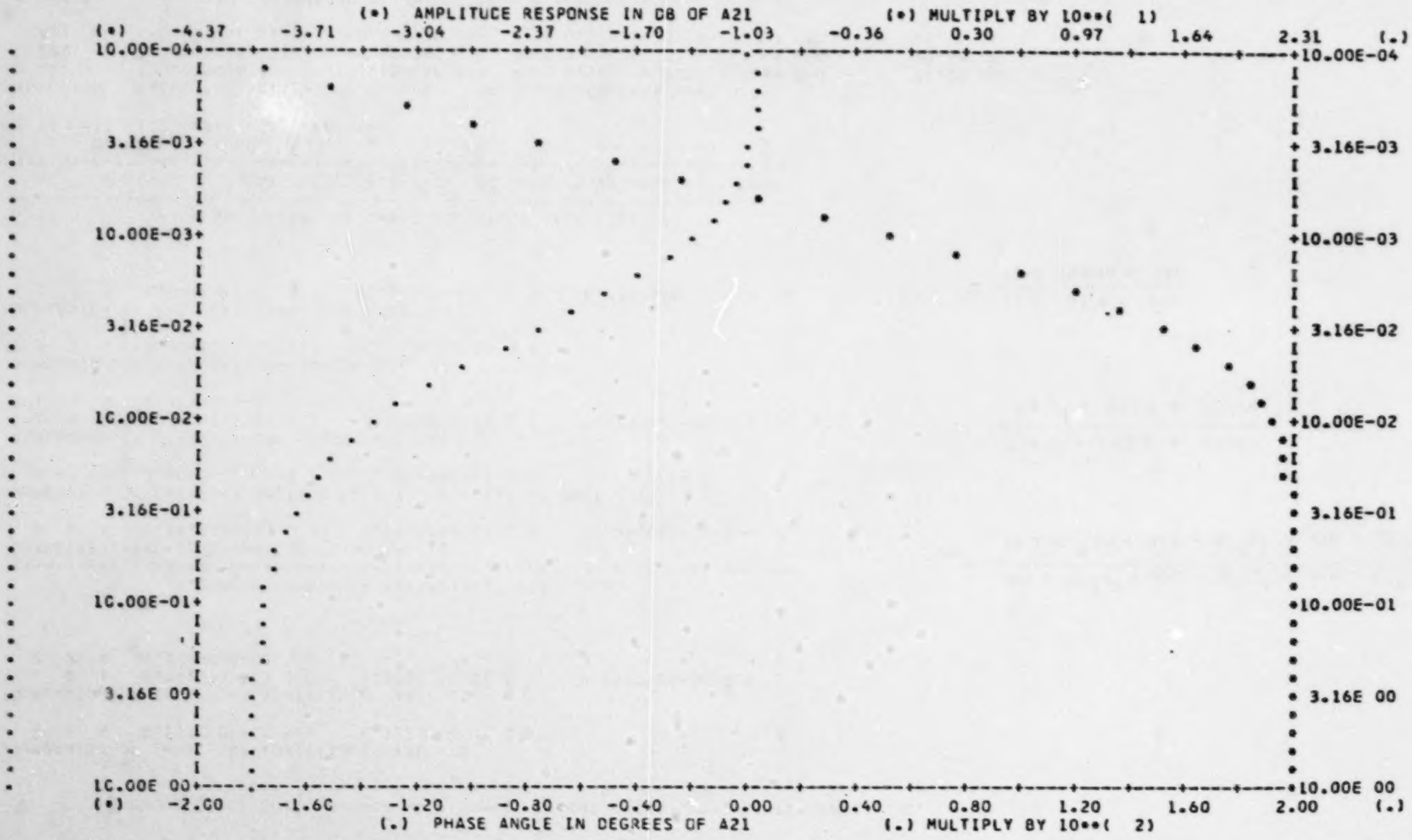
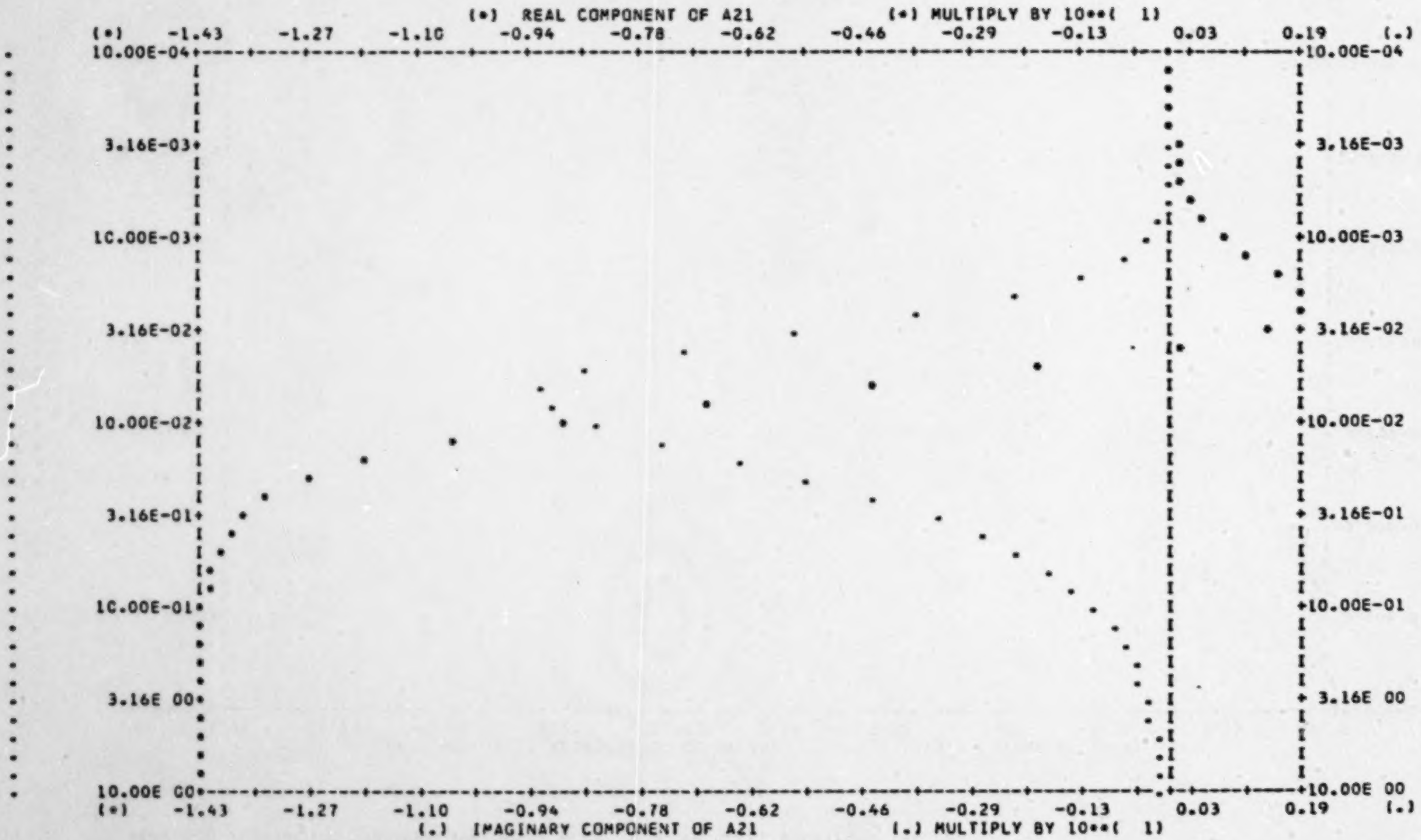
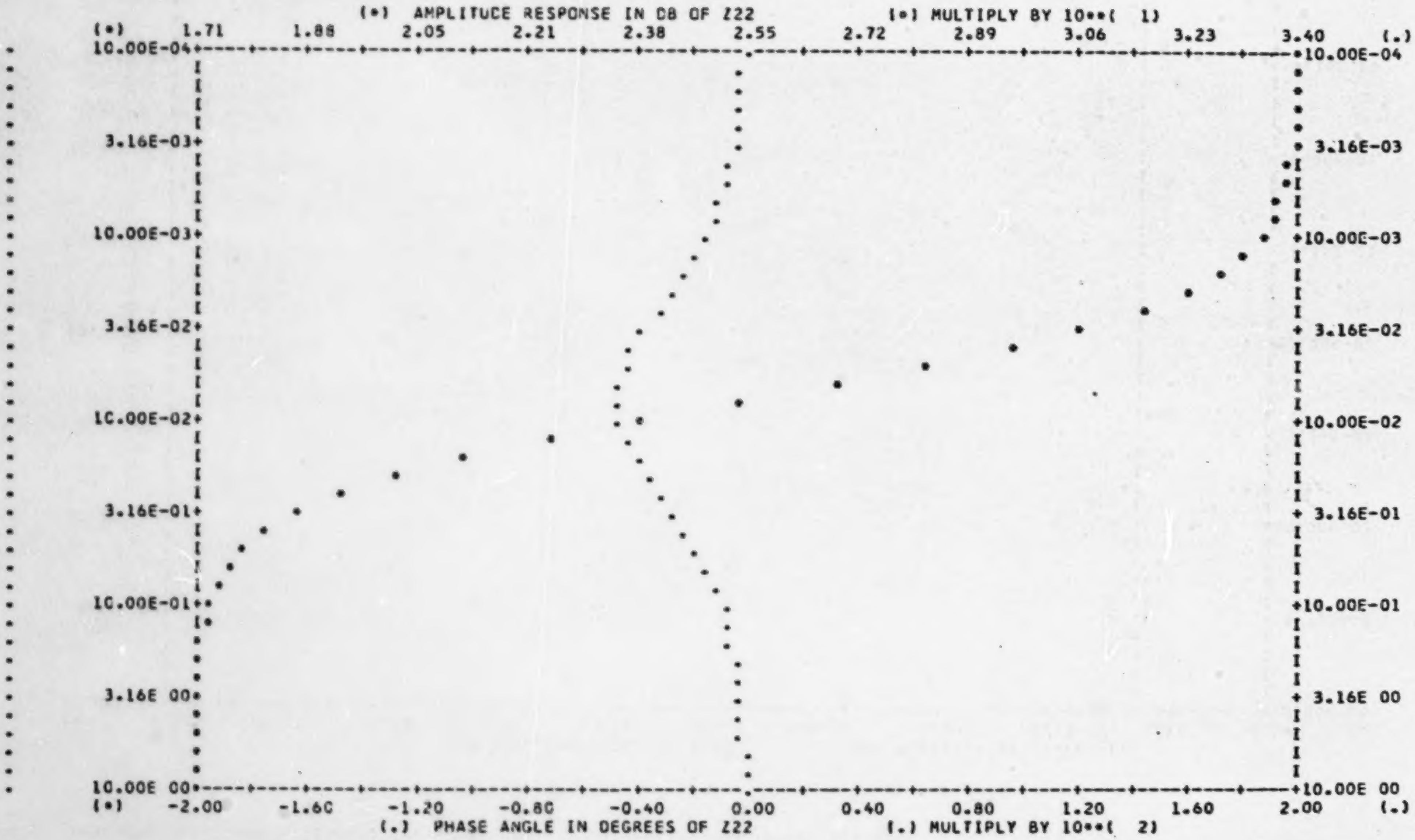
          FREQUENCY RESPONSE CHARACTERISTICS  (SR 1101)
--------------------------------------------------------------------
  L    F-MIN      F-MAX    EXP CPS NINCR LOG  AMPL GAIN ANGL REIM PRNT
=====================================================================
  2  0.001000  10.000000  -0   1   40    1    -0    1   -0    1   -0
  2  A21  Z22   -0   -0   -0   -0
```



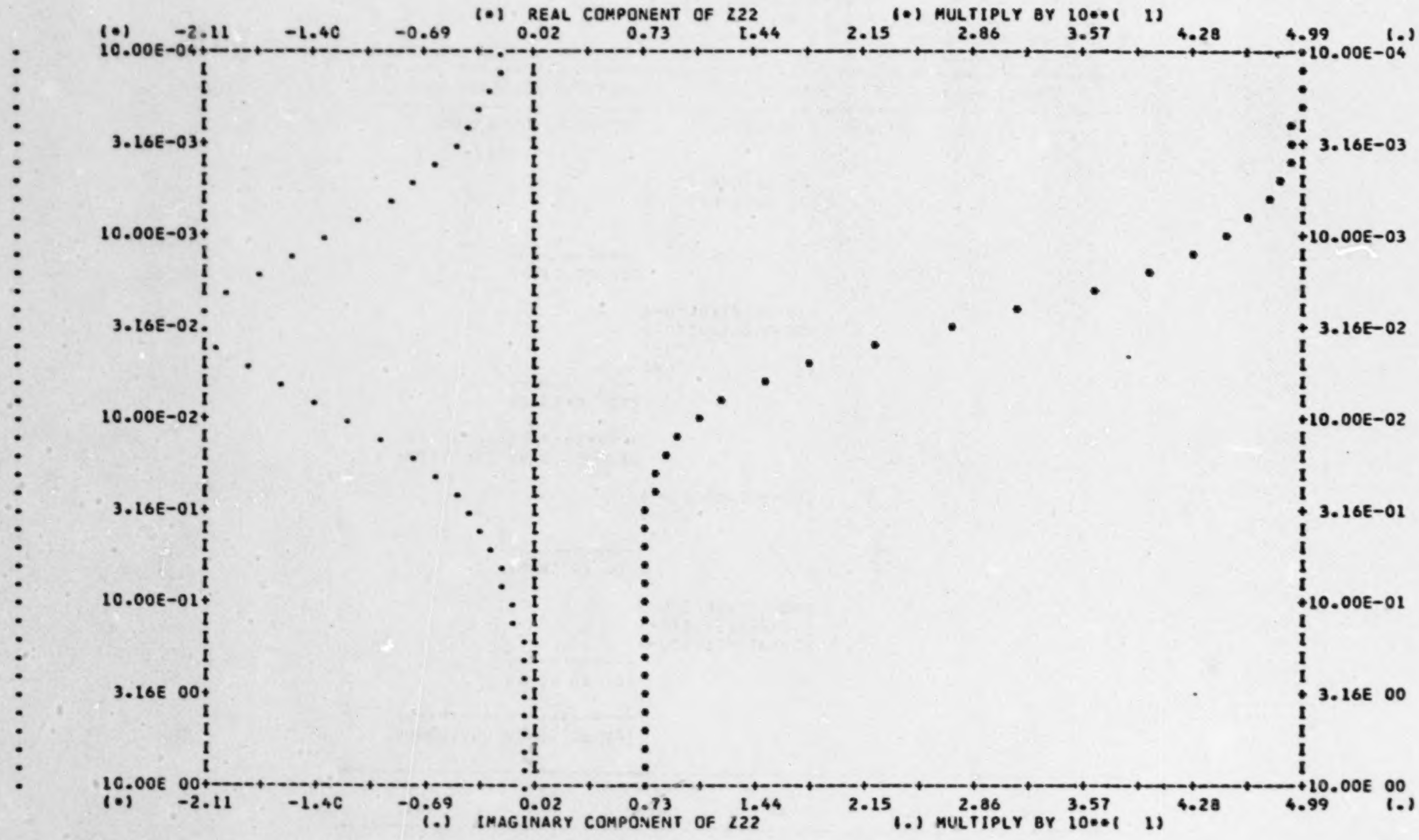
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.



HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.



HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.



```
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

                    ANALYSIS OF SYSTEM FUNCTIONS  (SR 1101)
--------------------------------------------------------------------------------
        AMN        AMN         AMN         AMN         AMN         AMN
        A21        Z22          00          00          00          00
--------------------------------------------------------------------------------

     POLES AND ZEROS OF A21
     =====================

              POLES OF A21
              ------------
                             (-0.1875901E-00)
                             (-0.3883848E-01)
                             (-0.3030302E-00)

              ZEROS OF A21
              ------------
                             (-0.           )
                             (-0.           )
                             (-0.2500000E-01)

     POLES AND ZEROS OF Z22
     =====================

              POLES OF Z22
              ------------
                             (-0.           )
                             (-0.           )
                             (-0.1875901E-00)
                             (-0.3883848E-01)

              ZEROS OF Z22
              ------------
                             (-0.           )
                             (-0.           )
                             (-0.1290479E 01)
                             (-0.3952019E-01)


           NODE-PAIR EQUATIONS.  (1/S FACTOR IS REMOVED.  SR 1102)
--------------------------------------------------------------------------------
  L  M NA  INVERSE INDUCTANCE    CONDUCTANCE              CAPACITANCE
================================================================================
  1  1  3   0.                S 0   0.              S 1   1.000000E-02 S 2  1
  6  1  3   0.                S 0   0.              S 1  -1.000000E-02 S 2  1
  2  2  3   0.                S 0   0.543030E 00    S 1   0.200000E 01 S 2  1
  3  2  2   0.                S 0  -0.200000E-01    S 1            +        1
  4  2  2   0.                S 0  -0.200000E-01    S 1            +        1
  5  2  3   0.                S 0  -0.500000E 00    S 1  -0.200000E 01 S 2  1
  6  2  2   0.                S 0  -0.303030E-02    S 1            +        1
  2  3  2   0.                S 0  -0.200000E-01    S 1            +        1
  3  3  3   0.                S 0   0.200000E-01    S 1   0.100000E-00 S 2  1
  4  3  3   0.                S 0   0.              S 1  -0.100000E-00 S 2  1
  2  4  2   0.                S 0  -0.200000E-01    S 1            +        1
  3  4  3   0.                S 0   0.              S 1  -0.100000E-00 S 2  1
  4  4  3   0.                S 0   0.120000E-00    S 1   0.100000E-00 S 2  1
  5  4  2   0.                S 0  -0.100000E-00    S 1            +        1
  2  5  3   0.            S 0   -0.500000E 00 S 1   -0.200000E 01 S 2  1
  4  5  2   0.            S 0   -0.210000E 01 S 1               +       1
  5  5  3   0.            S 0    0.260000E 01 S 1    0.200000E 01 S 2  1
  1  6  3   0.            S 0    0.             S 1   -1.000000E-02 S 2  1
  2  6  2   0.            S 0   -0.303030E-02 S 1               +       1
  4  6  2   0.            S 0    0.200000E 01 S 1               +       1
  5  6  2   0.            S 0   -0.200000E 01 S 1               +       1
  6  6  3   0.            S 0    0.303030E-02 S 1    1.000000E-02 S 2  1
--------------------------------------------------------------------------
NODE            CURRENT STEP     CURRENT IMPULSE     (EQUIVALENT SOURCES)
**************************************************************************
  2 -1  1  -0.600000E 01 S 0            +                      +        1
  4 -1  1   0.600000E 01 S 0            +                      +        1


             RESULTS OF DC MEASUREMENTS AT NODES  (SR 1102)
      ----------------------------------------------------------
       NODE NUMBER      VOLTAGE TO GROUND      INDUCTIVE CURRENT
      **********************************************************
              1               0.                    -0.
              2               0.                    -0.00000
              3               0.                    -0.
              4             152.94118                0.00000
              5               5.88235               -0.00000
              6               0.                    -0.


          RESULTS OF DC MEASUREMENT OF COMPONENTS  (SR 1102)
      ----------------------------------------------------------
       CMPNT  PORT   VOLTAGE      CURRENT       POWER   RATING
      **********************************************************
        G10     1      -5.882       0.           -0.      0.50 POWER
                2     147.059       2.941       432.526
        C 1     1       0.          0.            0.    200.00 VOLTS
        C 2     1      -5.882       0.            0.     20.00 VOLTS
        C 3     1     152.941       0.            0.    200.00 VOLTS
        R 1     1       0.          0.            0.      0.50 POWER
        R 2     1       5.882       2.941        17.301   0.50 POWER
        R 3     1    -152.941      -3.059       467.820   0.50 POWER
        R 4     1       0.          0.            0.      0.50 POWER


                TWO-PORT ADMITTANCE PARAMETERS  (SR 1102)
**************************************************************************
CHARACTERISTIC DENOMINATOR POLYNOMIAL IS
  0  0  4   0.791273E-01 S 0    0.648999E 00 S 1    0.143515E 01 S 2  2
  0  0  4   0.512000E 00 S 3            +                   +         2

NUMERATOR OF SHORT-CKT CURRENT (DUE TO SOURCES) AT PORT 2 IS
  2 -1  3   0.121018E 01 S 0    0.492451E 01 S 1    0.307200E 01 S 2  2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y11  IS
  1  1  4   0.791273E-03 S 1    0.387879E-02 S 2    0.155152E-02 S 3  2
```

```
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NUMERATOR OF SHORT-CKT ADMITTANCE  Y21  IS
  2  1  4   0.256000E-00 S 2    0.102400E 01 S 3              +       2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y22  IS
  2  2  4   0.158255E-02 S 0    0.208927E-01 S 1    0.734332E-01 S 2  2
  2  2  4   0.716800E-01 S 3              +                   +       2


                TWO-PORT IMPEDANCE PARAMETERS  (SR 1102)
=======================================================================
CHARACTERISTIC DENOMINATOR POLYNOMIAL IS
  0  0  5   0.158255E-04 S 2    0.156703E-03 S 3    0.217212E-03 S 4  3

NUMERATOR OF OPEN-CKT VOLTAGE (DUE TO SOURCES) AT PORT 2 IS
  2 -1  4   0.121018E-01 S 2    0.930909E-02 S 3              +       3

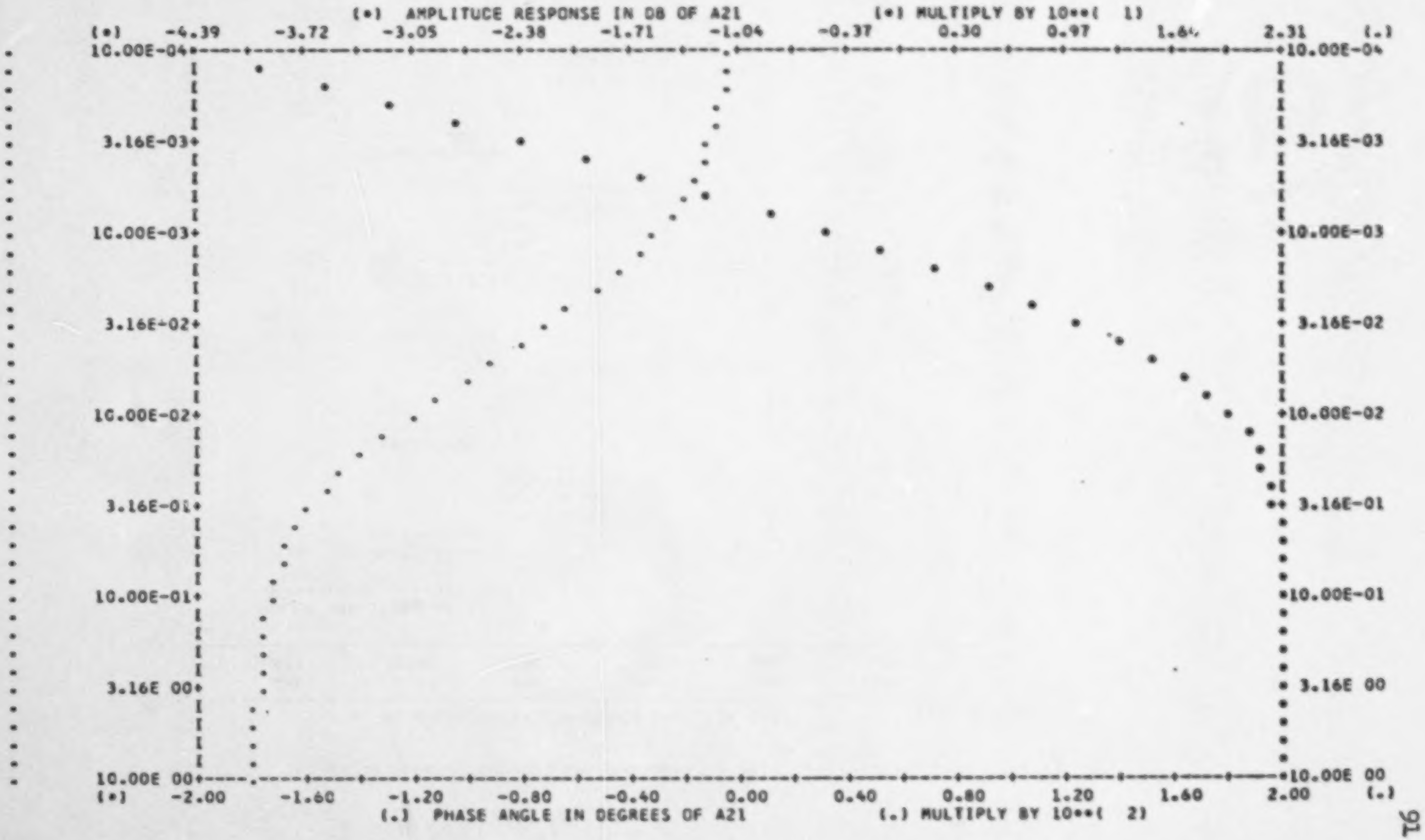
NUMERATOR OF OPEN-CKT IMPEDANCE  Z11  IS
  1  1  5   0.158255E-02 S 1    0.208927E-01 S 2    0.734332E-01 S 3  3
  1  1  5   0.716800E-01 S 4              +                   +       3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z21  IS
  2  1  5  -0.256000E-00 S 3   -0.102400E 01 S 4              +       3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z22  IS
  2  2  5   0.791273E-03 S 2    0.387879E-02 S 3    0.155152E-02 S 4  3


              FREQUENCY RESPONSE CHARACTERISTICS  (SR 1102)
-----------------------------------------------------------------------
   L    F-MIN      F-MAX   EXP CPS NINCR LOG  AMPL GAIN ANGL REIM PRNT
=======================================================================
   3   0.001000  10.000000 -0   1   40    1    -0    1   -0   -0   -0
   3  A21   -0   -0   -0   -0   -0
```

HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.



```
    HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

                 ANALYSIS OF SYSTEM FUNCTIONS  (SM 1102)
-------------------------------------------------------------------------
     AMN          AMN          AMN          AMN          AMN          AMN
     A21          Z22           00           00           00           00
-------------------------------------------------------------------------

     POLES AND ZEROS OF A21
     ======================

               POLES OF A21
               ------------
                            (-0.3030304E-00)
                            (-0.1214286E-00)
                            (-0.5999958E 00)

               ZEROS OF A21
               ------------
                            (-0.           )
                            (-0.           )
                            (-0.2500000E-00)

     POLES AND ZEROS OF Z22
     ======================

               POLES OF Z22
               ------------
                            (-0.           )
                            (-0.           )
                            (-0.6000001E 00)
                            (-0.1214286E-00)

               ZEROS OF Z22
               ------------
                            (-0.           )
                            (-0.           )
                            (-0.2275913E 01)
                            (-0.2240858E-00)
```

```
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

              I N V O I C E   F O R   E L E C T R O N I C   U N I T S   M A N U F A C T U R E D

 SOLD TO  JOBSHOP EXAMPLE            STUDENT IDENT. NUMBER   577            INVOICE DATE  5/13/65

 ITEM   YOUR ORDER  SERIAL              DESCRIPTION                          COST OF MANUFACTURE
NUMBER    NUMBER    NUMBER                                           PARTS    ASSEMBLY   TESTS      TOTAL

   1       1045      1101   CATHODE BI-PASSED TRIODE AMPLIFIER      230.89    102.65     19.40     352.94
   2       1045      1102   CATHODE BI-PASSED TRIODE AMPLIFIER      230.89     45.18     14.40     290.47
   3       1045      1103   CATHODE BI-PASSED TRIODE AMPLIFIER      230.89     31.75      6.30     268.94

                                                                     TOTAL AMOUNT OF INVOICE $     912.36
```

MODIFY

When NODE EQUATIONS (column 24 of the WORK ORDER card - front of the JOBSHOP coding form) has been entered as 2, you will receive, in addition to the printed data output you request, a deck of punched cards. Punched into columns 74-77 of these cards will be the serial number of the particular unit which these cards represent. In columns 79 and 80, the cards are consecutively numbered, beginning with 0. The first card (bearing the serial number of the unit and the identifying number 0 in column 80) is a partial copy of your original JOB card with the five 1's (ones) deleted from columns 1-5. There follows a group of cards, one for each non-zero element of the indefinite, or floating, admittance matrix for this unit of the design. The next-to-last card of this deck signifies that all of the matrix elements have been entered; it is blank except for + punched into columns 24, 44, and 64. The last card bearing the serial number of this unit is a cost accounting card; it is a record of the cost of parts, cost of assembly, and cost of tests invested in this unit up to the present time. Several more cards may follow those just described; they are not of interest in modifying a unit.

To modify a unit already constructed, you should proceed as follows. Either: make a copy of your original JOB card into which you punch 1 in column 72, the serial number of this unit in columns 74-77 and the number 0 in column 80; or: punch 1's (ones) in the first five columns of the first of the cards (the one with 0 punched in column 80) returned to you under the "punch NODE EQUATIONS" option you elected by entering 2 in column 24 of your original JOB card. Follow this card with a new WORK ORDER card. Directions for making out this card are the same as those for the original WORK ORDER card (see above) with the following exceptions:

a). The serial number of the unit to be modified must be entered in columns 67-70. This serial number may not be changed from the number assigned to this unit when it was first built.

b). The number 1 must be entered in column 72.

Next, enter all the rest of the cards returned to you bearing the serial number of this unit, starting with the card having 1 punched in column 80 and ending with the cost card as described in the previous paragraph. Follow these cards with COMPONENT cards (see section 3 above) which give the precise directions for the desired modification of the unit. If you enter here a COMPONENT card specifying a circuit element to be connected between a certain pair of nodes, the program will place the new element in parallel with whatever element(s) was(were) connected between those nodes in the unit as originally constructed. It is also possible to remove elements from the original circuit by specifying the negative of the original element. Suppose, for example, that the original design had a 50,000 ohm resistor and a .01 microfarad capacitor connected between nodes 5 and 7. If you entered a capacitor of -.01 microfarad from node 5 to node 7 on the modified unit, the new (or modified) circuit would have only the 50,000 ohm resistor between nodes 5 and 7. CAUTION: When non-zero tolerances are used, the various parameters will differ from the design values. Thus the probability that two (say ten percent) components, assigned equal but opposite (in sign) values will add to zero is remote.

Note that adding new elements in series creates new nodes. Suppose that you had a 50,000 ohm resistor connected from node 3 to node 6 and that TOTAL NUMBER NODES was 8. You could put a 2 millihenry inductor in series with this resistor by using three COMPONENT Cards as follows:

TYPE	NUMBER	I	J	HI
R	13	3	6	-50,000
R	14	3	9	50,000
L	11	6	9	.002

In this case, TOTAL NUMBER NODES (columns 2 and 3 of the WORK ORDER card) would have to be increased from 8 to 9.

After the last of the new component cards, enter the SNORM card, then PHASOR-FUNCTION card pairs, and POLE & ZERO cards in the same way as for the original design.

The invoice received for a modified unit will include all charges for the unit as originally constructed. That is, charges incurred in modifying a unit are added to the original invoice. For example, suppose that a certain unit contained $180.00 worth of parts, and that costs for construction and tests on that unit were $20.00 and $40.00, respectively. If you modify the unit to include $30.00 worth of new parts which cost $5.00 to install, and repeat the same tests as were made on the original unit, your invoice for the modified unit will include

PARTS	LABOR	TESTS
$210.00	$25.00	$80.00

NODE RENUMBERING

You may wish to rearrange the node numbers of a unit you have previously had constructed. To do so, use the procedure described above under MODIFY, with these exceptions.

a.) If the circuit contains an operational amplifier, the ground node may not be renumbered.

b.) On the WORK ORDER card, enter a 1 (one) in column 71 as well as a 1 in column 72. (Note that you may modify a unit by entering a 1 in column 72, nothing in column 71; however, if you enter a 1 in column 71, you must also enter 1 in column 72.

c.) Follow the WORK ORDER card with a card specifying how the node numbers are to be re-assigned (see below). Enter in column (2 and) 3 the number to be assigned to the node previously numbered 1; enter in column (5 and) 6 the number to be assigned to the node previously numbered 2.[1]

For example, a NODE RENUMBERING card made out as follows:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
		3			2			4			1			5		

(continued)

---

[1] For those who are familiar with FORTRAN, the format for this node renumbering card is 20I3.

$$\begin{array}{rcc} & \text{node number} & \text{to node} \\ \text{will change} & \left\{\begin{array}{c}1\\2\\3\\4\\5\end{array}\right. & \left.\begin{array}{c}3\\2\\4\\1\\5\end{array}\right\} \end{array}$$

ILLUSTRATION OF MODIFY

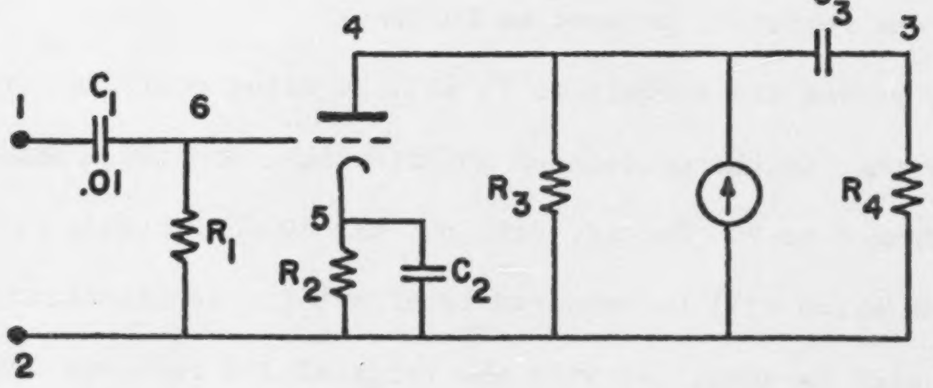
As an illustration of the MODIFY feature of JOBSHOP, consider again the example (page 70). In the original design for this amplifier, the power supply consisted of a 6-milliampere current source shunted by a 50,000-ohm resistor. To modify the circuit so that it employs the more usual (but equivalent) power supply made up of a 300-volt source in series with a 50,000-ohm resistor, proceed as follows.

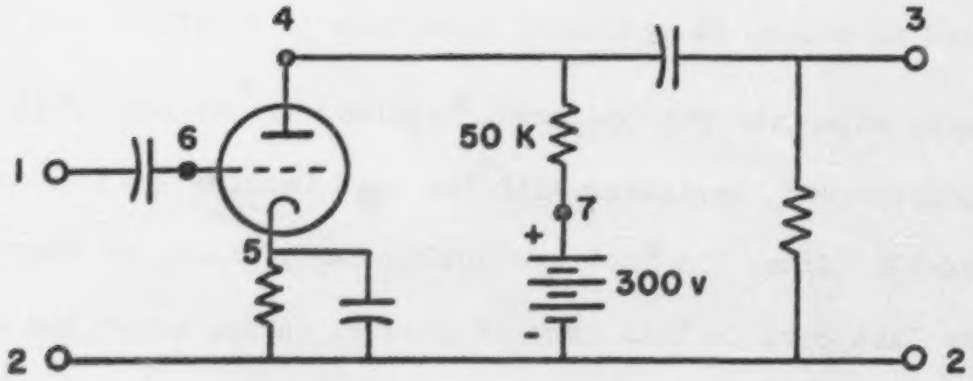
First, redraw the circuit as it will be after modification (figure IB3b). Notice that in the process of modification, the TOTAL NUMBER NODES is increased from 6 to 7. Second, fill out the JOBSHOP coding form, specifying the cards which will be required to effect the modification (figure IB4.) The JOB card is identical with the original JOB card for this unit. The WORK ORDER card has TOTAL NUMBER NODES entered as 7, in place of the 6 formerly entered there. The same outputs have been requested on this modified unit as on the original. The serial number, 1101, appearing in columns 67-70 agrees with the serial number of the unit originally built. The 1 entered in column 72 indicates that this is a MODIFY work order.

Next, enter the punched cards returned to you when unit 1101 was originally constructed, beginning with the card bearing the number 1101-01 in columns 74-80. After the cost accounting card, which, as described above, is the last card in this deck of punched cards, enter the COMPONENT cards which will be needed to effect the required changes. The first two COMPONENT cards remove the current source and its shunting resistor by adding their negatives in parallel with the original elements. The following two cards specify the voltage source and the series resistor; after these

Fig. I.B.3a

Fig. I.B.3b


C1
.01
1
6
4
C3
3
R1
5
R2
C2
R3
R4
2


4
3
1
6
50 K
7
+
300 v
-
5
2
2

cards, enter the SNORM card. In this example, the PHASOR-FUNCTION card pairs and POLE & ZERO cards entered with the original work order for serial number 1101 have been re-used, so that it has not been necessary to specify more cards on the back of the coding form.

Sample JOBSHOP print-out for illustrative example of MODIFY — the cathode by-pass triode amplifier

FIG. I.B.4. CODING FORM FOR MODIFIED CATHODE BY - PASSED AMPLIFIER

HOMEWOOD JOBSHOP CODING FORM

PAGE ______ OF ______ PAGES
DATE ______
IDENTIFICATION ______ 73 80

	STUDENT NUMBER	ORDER NUMBER	YOUR NAME	DESCRIPTION OF JOB	
1 1 1 1 1	577	1045	JOBSHOP--MODIFY	MODIFIED TRIODE AMPLIFIER	CARD JOB

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

TOTAL NUMBER NODES	INPUT NODE	OUTPUT NODE	GROUND NODE	LOT SIZE	COST PARTS	D.C. VALUES	NODE EQUATIONS	TWO-PORT Y PARAM.	TWO-PORT Z PARAM.	PHASORS	POLES & ZEROS	SERIAL NUMBER	MODIFY	
7	1	3	2	1	1	2	2	1	1	1	1	1101	1	ORDER

HI	HR
HF	HO

H - MATRIX

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

TYPE	NUMBER	I	J	K	L	TOL	RATING	MEXP	HI	HR	HF	HO	
R	13	4	2						-50.				COMPT
ST	12	4	2						6.0				
VS	10	7	2						300.				
R	15	4	7						50.				
													SNORM

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72

C-76

SEE BACK OF PAGE FOR PHASOR, FUNCTIONS, AND TRANSIENT SPECIFICATIONS

```
          HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

* * * * * * * * * * * * D A T A   I N P U T * * * * * * * * * * * * *
----------------------------------------------------------------------
1111  577 1045 JOBSHOP EXAMPLE   CATHODE BI-PASSED TRIODE AMPLIFIER
----------------------------------------------------------------------
ND IN OT GO LT  $ CC EG YS ZS FR TR                              SR MOD
 7  1  3  2  1  1  2  2  1  1  1  1                            1101  1
----------------------------------------------------------------------
TYPE NO  I  J  K  L TOL RTNG EXP    HI          HR         HF       HO
======================================================================
  R  13  4  2 -0 -0  0.  0.50 -0 -50.00000  -0.         -0.      -0.
 ST  12  4  2 -0 -0  0. -0.    -0   6.00000  -0.         -0.      -0.
 VS  10  7  2 -0 -0  0. -0.    -0 300.00000  -0.         -0.      -0.
  R  15  4  7 -0 -0  0.  0.50 -0  50.00000  -0.         -0.      -0.
    -0 -0 -0 -0 -0  0. -0.    -0   1.00000  -0.         -0.      -0.


                  COST OF PARTS SPECIFIED ON THIS JOB
      ----------------------------------------------------------
        TYPE     PARTS     NOMINAL   RATING    TOLERANCE    COST
                 NUMBER     VALUE
      ==========================================================
          R        13     -50.00000    0.500        0.       6.22
         ST        12       6.00000  -0.            0.       1.00
         VS        10     300.00000  -0.            0.       1.00
          R        15      50.00000    0.500        0.       6.22
      ----------------------------------------------------------
                       COST OF PARTS FOR ONE UNIT IS  $ 245.34


            NODE-PAIR EQUATIONS.  (1/S FACTOR IS REMOVED.  SR 1101)
----------------------------------------------------------------------
 L  M NA  INVERSE INDUCTANCE    CONDUCTANCE          CAPACITANCE
======================================================================
 1  1  3   0.                S 0    0.              S 1   1.000000E-02 S 2  1
 6  1  3   0.                S 0    0.              S 1  -1.000000E-02 S 2  1
 2  2  3   0.                S 0    0.523030E 00    S 1   0.200000E 02 S 2  1
 3  2  2   0.                S 0   -0.200000E-01    S 1          +          1
 4  2  2   0.                S 0    0.232831E-09    S 1          +          1
 5  2  3   0.                S 0   -0.500000E 00    S 1  -0.200000E 02 S 2  1
 6  2  2   0.                S 0   -0.303030E-02    S 1          +          1
 2  3  2   0.                S 0   -0.200000E-01    S 1          +          1
 3  3  3   0.                S 0    0.200000E-01    S 1   1.000000E-01 S 2  1
 4  3  3   0.                S 0    0.              S 1  -1.000000E-01 S 2  1
 2  4  2   0.                S 0    0.232831E-09    S 1          +          1
 3  4  3   0.                S 0    0.              S 1  -1.000000E-01 S 2  1
 4  4  3   0.                S 0    0.120000E-00    S 1   1.000000E-01 S 2  1
 5  4  2   0.                S 0   -1.000000E-01    S 1          +          1
 7  4  2   0.                S 0   -0.200000E-01    S 1          +          1
 2  5  3   0.                S 0   -0.500000E 00    S 1  -0.200000E 02 S 2  1
 4  5  2   0.                S 0   -0.210000E 01    S 1          +          1
 5  5  3   0.                S 0    0.260000E 01    S 1   0.200000E 02 S 2  1
 1  6  3   0.                S 0    0.              S 1  -1.000000E-02 S 2  1
 2  6  2   0.                S 0   -0.303030E-02    S 1          +          1
 4  6  2   0.                S 0    0.200000E 01    S 1          +          1
 5  6  2   0.                S 0   -0.200000E 01    S 1          +          1
 6  6  3   0.                S 0    0.303030E-02    S 1   1.000000E-02 S 2  1
 4  7  2   0.                S 0   -0.200000E-01    S 1          +          1
 7  7  2   0.                S 0    0.200000E-01    S 1          +          1
```

```
        HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.

--------------------------------------------------------------------------
NODE          CURRENT STEP      CURRENT IMPULSE      (EQUIVALENT SOURCES)
==========================================================================
  2 -1  1   0.119209E-06 S 0           +                        +       1
  4 -1  1  -0.119209E-06 S 0           +                        +       1

              RESULTS OF DC MEASUREMENTS AT NODES  (SR 1101)
        ---------------------------------------------------------
         NODE NUMBER     VOLTAGE TO GROUND      INDUCTIVE CURRENT
        =========================================================
              1               0.                     0.
              2               0.                    -0.00000
              3               0.                     0.
              4             152.94116                0.00000
              5               5.88235               -0.00000
              6              -0.00000                0.00000
              7             300.00000                0.

             RESULTS OF DC MEASUREMENTS OF VOLTAGE SOURCES
        ---------------------------------------------------------
        SOURCE     VOLTAGE       CURRENT         POWER        RATING
        =========================================================
         VS10    300.00000     -2.94118    -882.35301       -0.

            RESULTS OF DC MEASUREMENT OF COMPONENTS  (SR 1101)
        ---------------------------------------------------------
         CMPNT  PORT    VOLTAGE       CURRENT        POWER   RATING
        =========================================================
          R13    1      152.941       -3.059     -467.820    0.50 POWER
          R15    1     -147.059       -2.941      432.526    0.50 POWER


                    TWO-PORT ADMITTANCE PARAMETERS  (SR 1101)
==========================================================================
CHARACTERISTIC DENOMINATOR POLYNOMIAL IS
  0  0  4   0.395636E-01 S 0    0.116232E 01 S 1    0.418056E 01 S 2  2
  0  0  4   0.256000E 01 S 3           +                   +          2

NUMERATOR OF SHORT-CKT CURRENT (DUE TO SOURCES) AT PORT 2 IS
  2 -1  3  -0.120221E-07 S 0  -0.132150E-06 S 1  -0.305176E-06 S 2  2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y11  IS
  1  1  4   0.395636E-03 S 1    0.103176E-01 S 2    0.775757E-02 S 3  2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y21  IS
  2  1  4   0.128000E-00 S 2    0.512000E 01 S 3               +      2

NUMERATOR OF SHORT-CKT ADMITTANCE  Y22  IS
  2  2  4   0.791273E-03 S 0    0.272027E-01 S 1    0.189758E-00 S 2  2
  2  2  4   0.358400E-00 S 3           +                   +          2
```

```
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.


                TWO-PORT IMPEDANCE PARAMETERS  (SR 1101)
======================================================================
CHARACTERISTIC DENOMINATOR POLYNOMIAL IS
  0  0  5   0.791273E-05 S 2    0.245915E-03 S 3    0.108606E-02 S 4  3

NUMERATOR OF OPEN-CKT VOLTAGE (DUE TO SOURCES) AT PORT 2 IS
  2 -1  4  -0.120221E-09 S 2   -0.924775E-09 S 3              +        3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z11  IS
  1  1  5   0.791273E-03 S 1    0.272027E-01 S 2    0.189758E-00 S 3  3
  1  1  5   0.358400E-00 S 4              +                   +        3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z21  IS
  2  1  5  -0.128000E-00 S 3   -0.512000E 01 S 4              +        3

NUMERATOR OF OPEN-CKT IMPEDANCE  Z22  IS
  2  2  5   0.395636E-03 S 2    0.103176E-01 S 3    0.775757E-02 S 4  3


               FREQUENCY RESPONSE CHARACTERISTICS  (SR 1101)
----------------------------------------------------------------------
   L    F-MIN      F-MAX   EXP CPS NINCR LOG  AMPL GAIN ANGL REIM PRNT
======================================================================
   1   0.100000   1.000000 -0   1    2   -0    -0   -0   -0   -0    1
   1  Z11  Z22  A21   -0   -0   -0

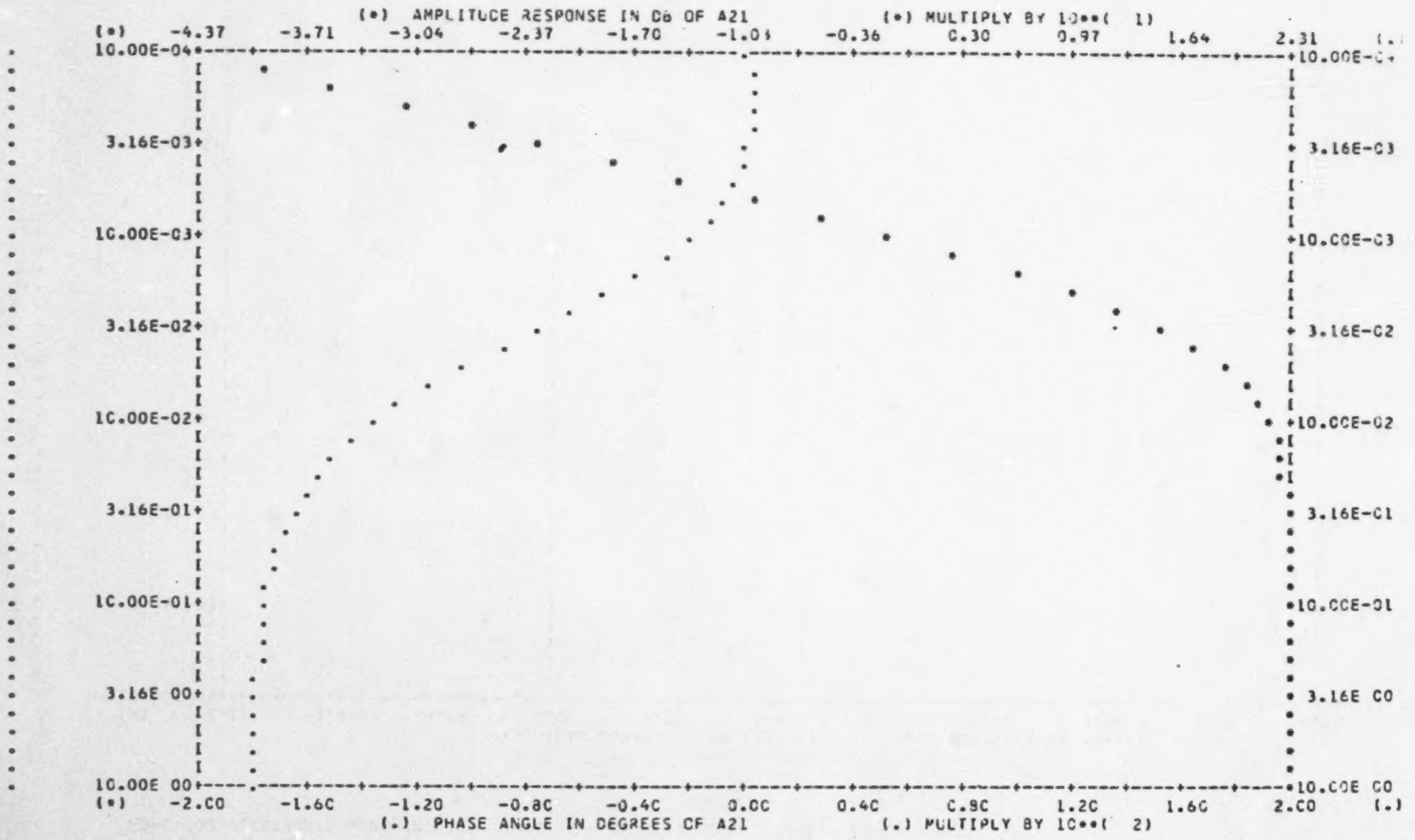
FUNCTION    VALUE AT   0.628319E 00 RPS    OR   1.000000E-01 CPS
  Z11       ( 0.33000E 03) + J(-0.15915E 03)  =  ( 0.36637E 03)/ -25.75 DEG        51.28 DB.
  Z22       ( 0.10568E 02) + J(-0.11524E 02)  =  ( 0.15636E 02)/ -47.43 DEG        23.88 DB.
  A21       (-0.89144E 01) + J(-0.84979E 01)  =  ( 0.12316E 02)/-136.37 DEG        21.81 DB.

FUNCTION    VALUE AT   0.345575E 01 RPS    OR   0.550000E 00 CPS
  Z11       ( 0.33000E 03) + J(-0.28937E 02)  =  ( 0.33127E 03)/  -5.01 DEG        50.40 DB.
  Z22       ( 0.72658E 01) + J(-0.22744E 01)  =  ( 0.76135E 01)/ -17.38 DEG        17.63 DB.
  A21       (-0.14059E 02) + J(-0.20630E 01)  =  ( 0.14210E 02)/-171.65 DEG        23.05 DB.

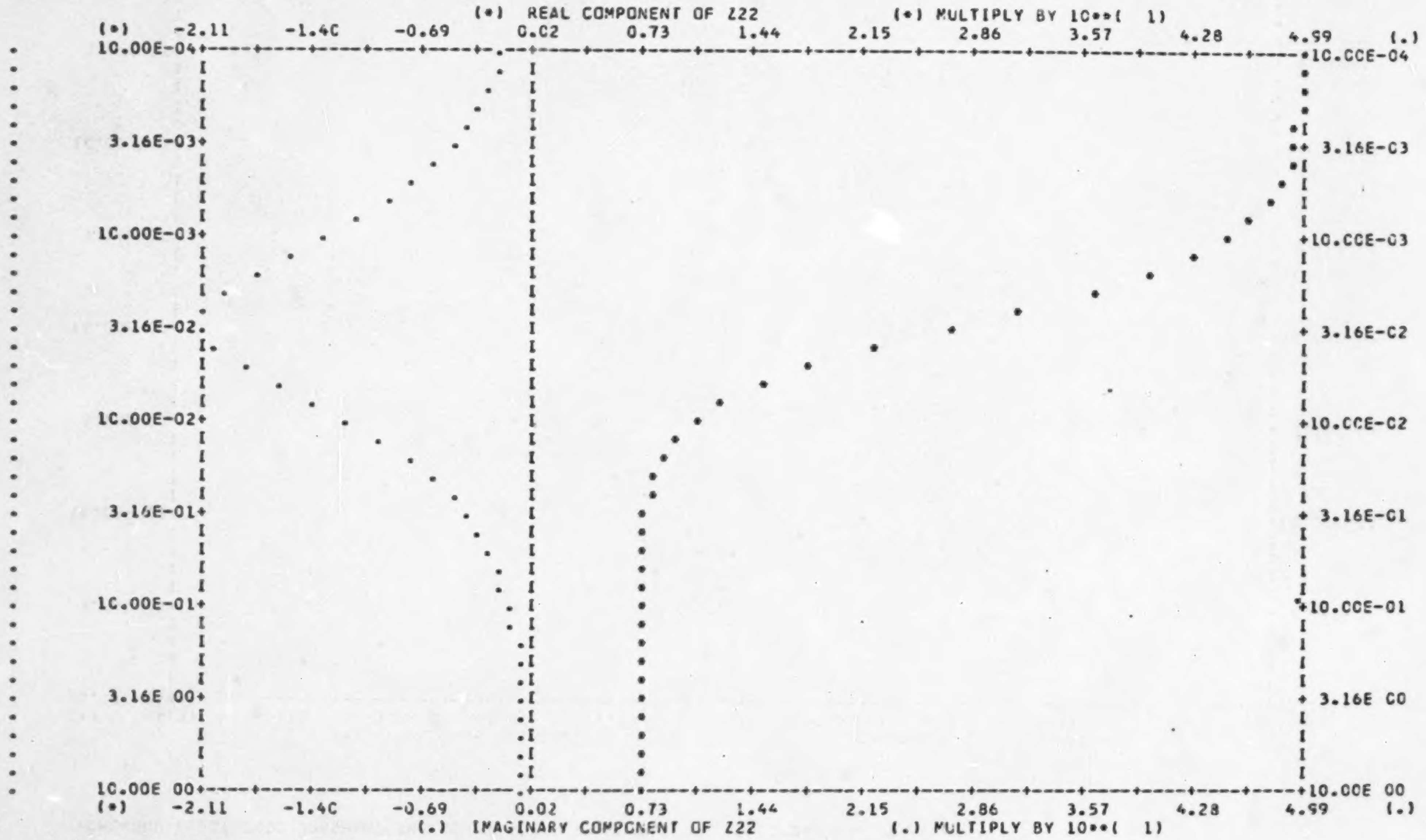
FUNCTION    VALUE AT   0.628319E 01 RPS    OR   1.000000E 00 CPS
  Z11       ( 0.33000E 03) + J(-0.15915E 02)  =  ( 0.33038E 03)/  -2.76 DEG        50.38 DB.
  Z22       ( 0.71801E 01) + J(-0.12535E 01)  =  ( 0.72887E 01)/  -9.90 DEG        17.25 DB.
  A21       (-0.14217E 02) + J(-0.11432E 01)  =  ( 0.14263E 02)/-175.40 DEG        23.08 DB.


               FREQUENCY RESPONSE CHARACTERISTICS  (SR 1101)
----------------------------------------------------------------------
   L    F-MIN      F-MAX   EXP CPS NINCR LOG  AMPL GAIN ANGL REIM PRNT
======================================================================
   2   0.001000  10.000000 -0   1   40    1    -0    1   -0    1   -0
   2  A21  Z22   -0   -0   -0   -0
```

HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 13, MD.



HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.



```
HOMEWOOD ELECTRONIC JOBSHOP, THE JCHNS HCPKINS UNIVERSITY, BALTIMORE 18, MC.

            I N V O I C E   F O R   E L E C T R C N I C   U N I T S   M A N U F A C T U R E D

 SOLC TO  JOBSHOP EXAMPLE          STUCENT ICENT. NUMBER   577           INVOICE CATE  5/18/65

 ITEM   YCUR CRCER  SERIAL              DESCRIPTION                        COST OF MANUFACTURE
NUMBER    NUMBER    NUMBER                                        PARTS   ASSEMBLY   TESTS     TOTAL

   1       1045      1101    CATHCOE BI-PASSEC TRIOCE AMPLIFIER    245.34   100.64     33.90    379.88

                                                                  TOTAL AMCUNT OF INVOICE $   379.88
```

ENTERING OTHER THREE- AND FOUR-TERMINAL ELEMENTS

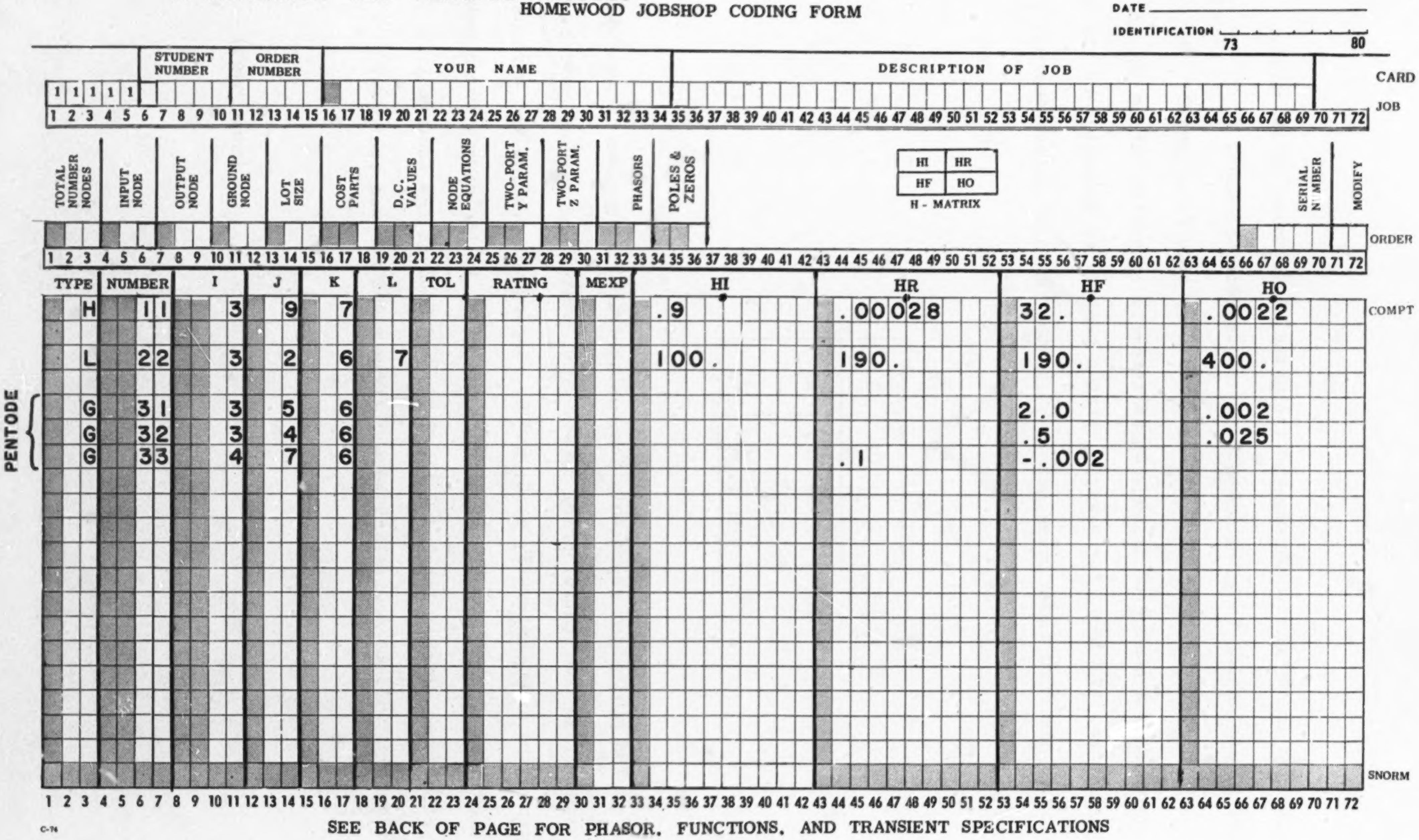
Figure IB5 is a reproduction of a section of the JOBSHOP coding form illustrating how certain other types of elements may be entered into the JOBSHOP program. Consider first, a junction transistor, connected in the common emitter configuration and represented by its H parameters. Suppose that HI, the input resistance, is 900 ohms; HR, the reverse voltage transfer ratio, is 2.8×10^{-4}; HF, the forward current transfer ratio, is 32; and HO, the output admittance, is 2200 micromhos. In the unit system in which the unit of resistance is the kilohm and the unit of conductance is the millimho, these numbers are:

HI = 0.9, HR = .00028, HF = 32, and HO - 0.0022

Thus if the node numbers 3, 7, and 9 have been assigned, respectively, to the base, emitter, and collector of the transistor, the element may be entered as shown on the line specifying H 11 on the accompanying reproduction of the coding form. This model may be further improved by adding a voltage source between the base and emitter nodes to represent the (nearly) constant base-to-emitter voltage.

Transformers may be entered as inductance two-port devices. Here, the parameters to be entered are the primary inductance, the secondary inductance, and the mutual inductance, which, it will be remembered, is given by $L_m = k\sqrt{L_1L_2}$ where the magnitude of the coupling coefficient, k, is less than or equal to 1 (one). The JOBSHOP program requires, however, that k be less than one. The transformer specified as L 22 on the accompanying coding form has primary terminals 3 and 6, secondary terminals 2 and 7; the primary inductance is 100 millihenries, the secondary

FIG. I.B.5. PARTIAL REPLICA OF CODING FORM ILLUSTRATING ENTRY OF TRANSISTOR, TRANSFORMER AND PENTODE MODELS



HOMEWOOD JOBSHOP CODING FORM

PAGE ______ OF ______ PAGES
DATE ______
IDENTIFICATION ______ 73 80

1 1 1 1 1	STUDENT NUMBER	ORDER NUMBER	YOUR NAME	DESCRIPTION OF JOB	CARD
1 2 3 4 5	6 7 8 9 10	11 12 13 14 15	16 … 34	35 … 69	70 71 72 JOB

TOTAL NUMBER NODES	INPUT NODE	OUTPUT NODE	GROUND NODE	LOT SIZE	COST PARTS	D.C. VALUES	NODE EQUATIONS	TWO-PORT Y PARAM.	TWO-PORT Z PARAM.	PHASORS	POLES & ZEROS	H - MATRIX: HI HR / HF HO	SERIAL NUMBER	MODIFY

ORDER

	TYPE	NUMBER	I	J	K	L	TOL	RATING	MEXP	HI	HR	HF	HO	
	H	11	3	9	7					.9	.00028	32.	.0022	COMPT
	L	22	3	2	6	7				100.	190.	190.	400.	
PENTODE	G	31	3	5	6							2.0	.002	
	G	32	3	4	6							.5	.025	
	G	33	4	7	6						.1	-.002		
														SNORM

C-74

SEE BACK OF PAGE FOR PHASOR, FUNCTIONS, AND TRANSIENT SPECIFICATIONS

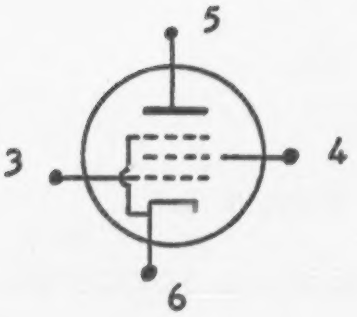
inductance is 400 millihenries, and the mutual inductance is 190 millihenries, indicating that the coefficient of coupling is 0.95.

Multigrid vacuum tubes may be entered by specifying the G parameters of a number of triodes whose totality is equivalent to the more complex tube. Suppose, for example, that a pentode is described by its G matrix in the form shown below, where ρ is the ratio of screen current to plate current.

$$\begin{array}{c|c|c|c|}
 & V_g & V_p & V_s \\
\cline{2-4}
i_g & 0 & 0 & 0 \\
\cline{2-4}
i_p & g_m & g_p & g_s \\
\cline{2-4}
i_s & \rho g_m & g_p & \rho g_s \\
\cline{2-4}
\end{array}$$

The equivalent representation, using triodes, is given below. In particular, if the control grid, screen grid, plate, and cathode have been assigned the node numbers 3, 4, 5, and 6, respectively, while the various conductances of the tube (in millimhos) are given in the matrix shown below, then the three triodes labeled G 31, G 32, and G 33 on the accompanying coding form, will be equivalent to the given model for the pentode.

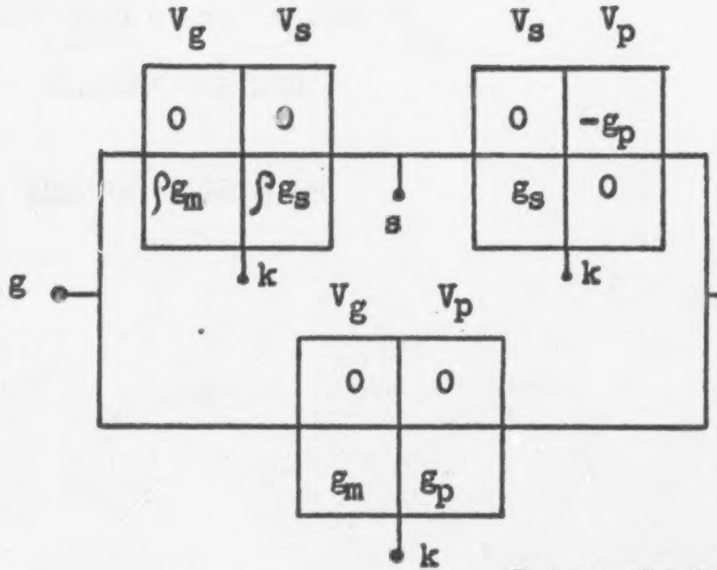
(continued)



Schematic

	V_g	V_p	V_s
ig	0	0	0
ip	g_m	g_p	g_s
is	ρg_m	$-g_p$	ρg_s

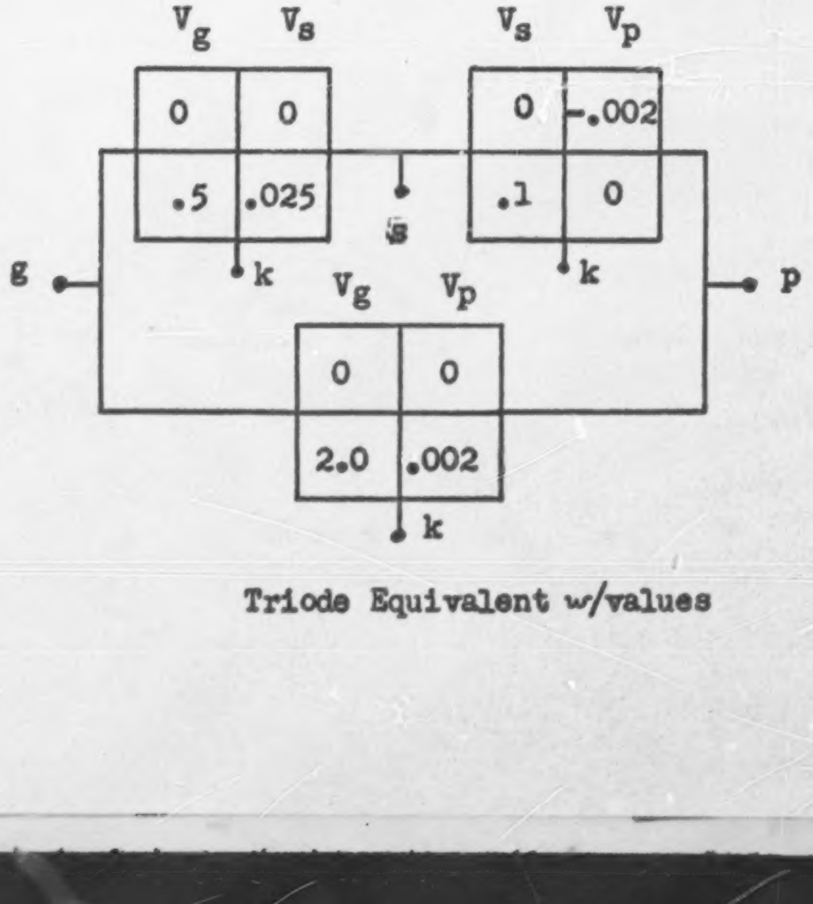
Model


V_g
V_s
0
0
ρg_m
ρg_s
s
k
V_s
V_p
0
$-g_p$
g_s
0
k
g
p
V_g
V_p
0
0
g_m
g_p
k

Triode Equivalent

	V_g	V_p	V_s
ig	0	0	0
ip	2.0	.002	.1
is	.5	-.002	.025

Typical Values


V_g
V_s
0
0
.5
.025
s
k
V_s
V_p
0
-.002
.1
0
k
g
p
V_g
V_p
0
0
2.0
.002
k

Triode Equivalent w/values

SECTION I.C

A MATHEMATICAL DESCRIPTION OF THE HOMEWOOD ELECTRONIC JOBSHOP PROGRAM

by ROBERT RATHBUN

SECTION I.C.

MATHEMATICAL DESCRIPTION OF THE JOBSHOP PROGRAM

JOBSHOP is a computer program to analyse electrical circuits. The user (i.e.the designer) specifies the configuration of his circuit to the program by means of data cards. This information is then used to construct a mathematical model of the specified circuit. Upon the mathematical model, any combination of the following tests may be performed:

1. The model is compressed, yielding two equations which describe the current-voltage relationships at the input terminals and at the output terminals of the specified circuit.
2. The dc operating conditions are determined.
3. The frequency response is computed and plotted.
4. The natural frequencies are calculated.

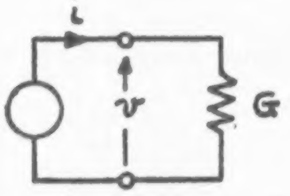
It is the purpose of this paper to discuss the basic principles and techniques incorporated in JOBSHOP. For this reason, very little is mentioned concerning how the program itself is used; information of this type is found in Sections I.A. and I.B.

Algebraic Representation of Circuit Elements and Signals. With a function f there is associated a function F which describes the behavior of f in the complex-frequency domain. The function F is the Laplace transform of f and is defined as:

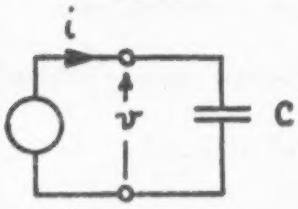
$$F(s) = \int_0^\infty f(t)\, e^{-st}\, dt.$$

It is easily shown from the definition that s may be considered as the differentiator operator and s^{-1} as the accumulator or integrator operator. That is, if f has the transform F, then f' has the transform sF. Likewise, if f' has the transform F, then f has the transform $\frac{F}{s}$.

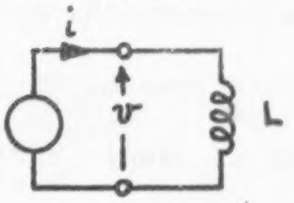
Because of the algebraic nature of the variable s, it is often convenient to disguise a system of simultaneous linear differential equations as a system of simultaneous linear equations in the variable s. Of particular relevance here is the use of s in describing the behavior of the circuit elements. Thus, the operators which relate the voltage and current are replaced by algebraic functions in the variable s, viz:



$$i = Gv \Rightarrow I = GV$$



$$i = C\frac{dv}{dt} \Rightarrow I = CsV$$



$$i = \frac{1}{L}\int v\,dt \Rightarrow I = \frac{1}{Ls}V$$

The admittance of an element (that is, the ratio $\frac{I}{V}$) is not a simple real number in all cases, but rather an operator in the variable s. For the above elements, the admittances are G, Cs, and $\frac{1}{Ls}$.

Similarly, by evaluating the above integral, one may show that the Laplace transforms for various time functions are:

	$f(t)$	$F(s)$
unit impulse	$\delta(t)$	1
unit step	1 for $t > 0$ $1/2$ for $t = 0$ 0 for $t < 0$	$1/s$
linearity	$c_1f_1+c_2f_2$	$c_1F_1+c_2F_2$

Notion of the Equivalent Two-port. The basis of JOBSHOP is the fundamental node-voltage method of analyzing electrical circuits. The designer specifies to the program a description of his circuit (that is, he specifies each component, its orientation, and its characteristic parameters) and also the three nodes which are to be the input-, the output-, and the ground-node. This information is used to establish a system of simultaneous linear equations; the system then describes the behavior of the circuit. In particular, a circuit containing n+1 nodes has an associated system of n independent equations. If the index 1 designates the input-node, the index 2 the output-node, and the index n+1 the ground-node, then the n equations, known as the node-equations, are each of the form:

$$I_k = g_{k1}E_1 + g_{k2}E_2 + \dots + g_{kn}E_n \quad (k = 1, 2, \dots, n)$$

where the symbols are defined as follows:

I_k is the current impressed, by sources, on node k,

E_i is the voltage at node i, measured with respect to the ground-node, and

g_{ki} is the operator-coefficient which relates the voltage at node i to the current leaving node k through linear circuit elements attached thereto.

The configuration of the circuit under consideration and the value of the components determine these operator-coefficients. Once the operator-coefficients have been determined and the system of node-equations has been established, an iterative procedure may be used to eliminate from the equations the "internal" variables E_3, E_4, ..., E_n. The procedure is the familiar one: the n-th equation is solved for E_n and the resultant expression is substituted into the remaining n-1 equations; there are now n-1 equations which depend on the variables $E_1, E_2, \ldots, E_{n-1}$; the solution-substitution process is applied to these n-1 equations, and so on, until there remain only two equations, each of which depends only on the input and output variables E_1 and E_2. The two equations resulting from the iterative procedure are:

$$I_1 = y_{11}E_1 + y_{12}E_2$$

$$I_2 = y_{21}E_1 + y_{22}E_2$$

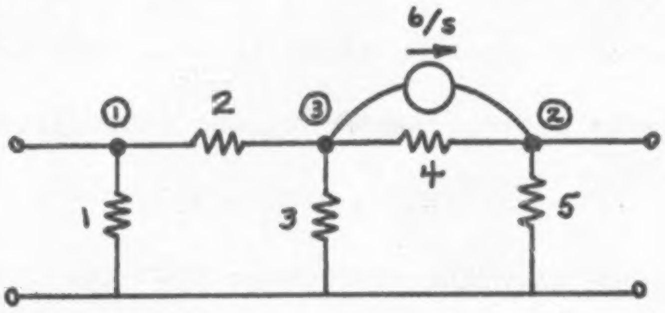
These equations, known as the admittance equations, describe the voltage-current relationship of the circuit at its input-node and at its output-node just as accurately as the original system of n equations. These two equations therefore define an equivalent two-port of the specified circuit; the terminology is justified by the following observations:

1) the variables E_1 and E_2 of the admittance equations are identical to the values of the voltages E_1 and E_2 of the specified circuit.
2) three-terminal elements, which constitute a class of two-port circuits, have an original system of equations which is identical to its admittance equations.

From Circuit to Node-equations. As mentioned, the operator-coefficients g_{ik} of the node-equations depend upon the circuit at hand, but nevertheless the equations themselves may be formed for any circuit by various systematic methods. One of these methods follows directly from application of

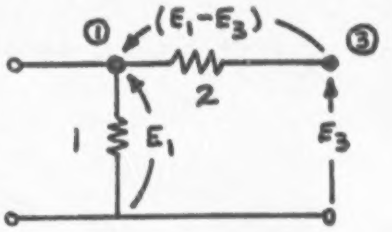
Kirchhoff's current law at each of the nodes of the circuit: for each node, except for the ground-node, there is written an equation which states that the current impressed upon the node is equal to the current leaving that node through the components attached to it. The following example illustrates this method.

The diagram represents the circuit to be examined:



(mhos, amperes)

The diagram of the circuit at node 1 is reproduced below:

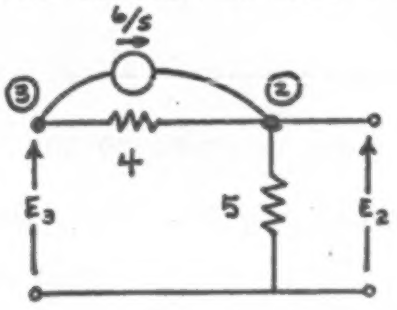


Because there are no sources attached to node 1, there is no current impressed on that node by sources; hence $I_1 = 0$. The current leaving node 1 through the components is simply the sum of the currents leaving through each of the components; this current is represented by the expression $(1\,E_1) + 2(E_1 - E_3)$. By Kirchhoff's law, the current impressed upon this node is equal to the current leaving it; that is:

$$0 = (1\,E_1) + 2(E_1 - E_3), \text{ or}$$

$$0 = 3E_1 - 2E_3.$$

The diagram of the circuit at node 2 is reproduced:



In this case, there is a source attached to the node, and it impresses a current of 6 amperes; hence $I_2 = 6$. The current leaving node 2 through the components is represented by the expression

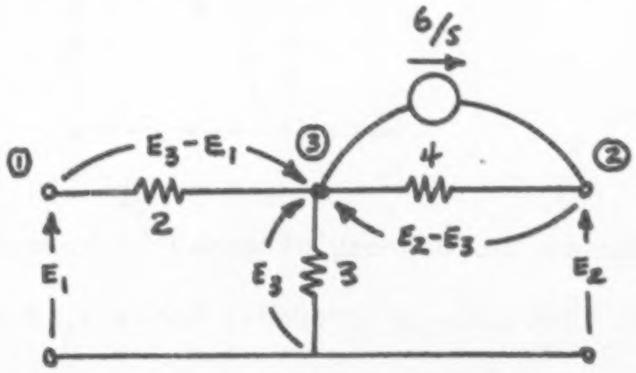
$$5(E_2) + 4(E_2 - E_3).$$

By the same law, these currents are equal; that is:

$$6/s = (5\ E_2) + 4(E_2 - E_3), \text{ or}$$

$$6/s = 9E_2 - 4E_3.$$

Finally, the circuit at node 3 is considered, with the diagram reproduced below:



The equation, which is obtained in the same manner as the previous ones, is:

$$-6/s = -2E_1 - 4E_2 + 9E_3.$$

When considered simultaneously, these equations form the system of node-equations for this circuit; that is, the system is the following set of equations:

$$0/s = 3E_1 \qquad - 2E_3$$

$$6/s = \qquad 9E_2 - 4E_3$$

$$-6/s = -2E_1 - 4E_2 + 9E_3.$$

From Node-equation to Equivalent Two-port. The example is continued, illustrating the iterative procedure used to determine the admittance equations.

In this case, only the variable E_3 must be eliminated from the system of equations, to obtain the admittance equations. The last of the above equations is rearranged, to express the dependence of E_3 upon the variables E_1 and E_2. The result is the expression:

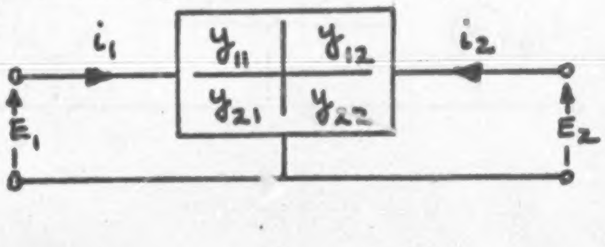
$$E_3 = \frac{1}{9}\left(-6/s + 2E_1 + 4E_2\right)$$

This expression is then substituted into the first and second equations, and the terms are rearranged to yield the admittance equations of the circuit:

$$-\frac{12}{9s} = \frac{23}{9}E_1 - \frac{6}{9}E_2$$

$$\frac{30}{9s} = -\frac{8}{9}E_1 + \frac{65}{9}E_2$$

The notion of the equivalent two-port is easily grasped if a special symbol is used to represent this electrical device. The symbol frequently used is the following:

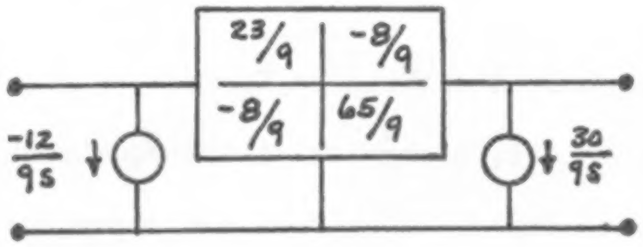


The symbol is but a short-hand representation of the equations which the device must satisfy; namely:

$$i_1 = y_{11} E_1 + y_{12} E_2$$

$$i_2 = y_{21} E_1 + y_{22} E_2$$

Using this symbol, the equivalent two-port of the circuit just considered may be represented as follows:

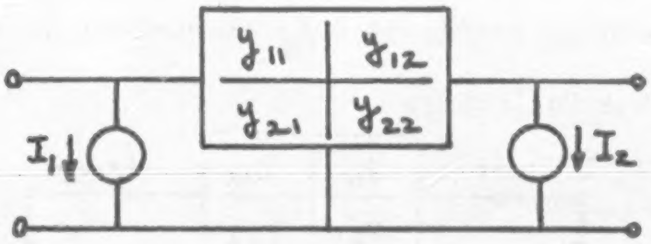


In this case it was necessary to supplement the special symbol with two current sources to account for the effect of the internal sources at the output-terminals. In general, any circuit which JOBSHOP handles can be represented, after its admittance equations have been found, as a combination of one two-port device and two current sources. This follows from the fact that the admittance equations are always of the form:

$$I_1 = y_{11} E_1 + y_{12} E_2$$

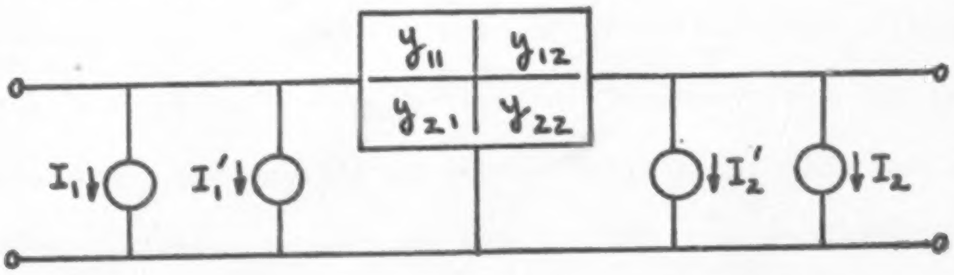
$$I_2 = y_{21} E_1 + y_{22} E_2$$

This implies that the equivalent two-port is always of the form:



The parameters y_{ik} account for that portion of the terminal current which is proportional to the terminal voltages, whereas I_1 and I_2 represent the terminal currents obtained when *both* terminal voltages are zero. The latter condition is obtained by short-circuiting the terminals; hence the y_{ik} are called the *short-circuit admittance parameters*, and the sources I_1 and I_2 are called the *Norton equivalent current sources*. The representation itself is known as the *Norton equivalent two-port*.

Equivalent Sources. Except in the case of extremely degenerate circuits, the two-port device must always be supplemented with Norton equivalent sources whenever sources appear within the original circuit. These equivalent sources account for the current sources within the original circuit. Likewise, to account for non-zero *initial conditions*, the two-port device may be supplemented with two *additional* current sources. To allow comparison, the equivalent sources arising from the internal sources are kept separate from the equivalent sources arising from non-zero initial conditions. The two-port representation which accounts for both is then:



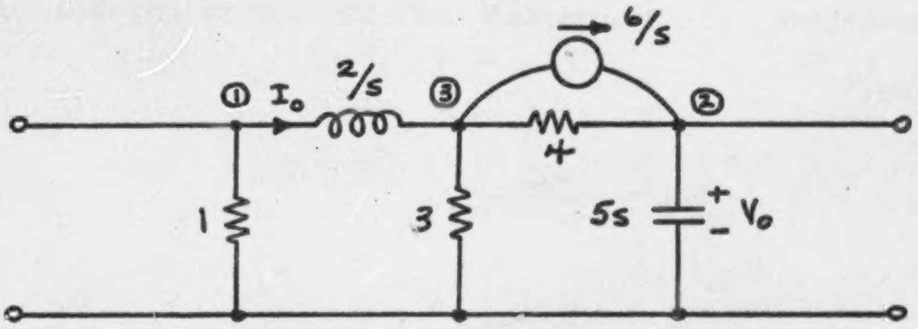
The sources I_1' and I_2' account for non-zero initial conditions, and the sources I_1 and I_2 account for the internal sources.

The initial condition is a state of being, not a circuit element. How then can a state of being be described in a system of equations, the terms of which arise solely from the appearance of circuit elements? The answer is that the initial condition itself is not considered, but rather the most simple cause of the condition; that is, each element with non-zero initial condition is replaced with an identical element in combination with some current source whose value is determined by the value of the initial condition it is to induce. Thus, it may be assumed that each circuit contains two types of sources: one type consisting of the original sources as specified by the designer; and the other type consisting of the sources needed to cause the initial conditions.

Because the circuits under consideration are linear, the principle of superposition may be applied in determining the value of these two types of equivalent sources. First, the circuit is treated as though all initial conditions were zero; that is, the values of the sources needed to cause the initial conditions are set to zero, and only the sources specified by the designer are considered. The admittance equations of this circuit are then found, and the values of the equivalent sources I_1 and I_2 are extracted. Next, the circuit is treated as though there were no internal sources; that is, the values of the sources specified by the designer are set to zero, and only the sources needed to account for the non-zero initial conditions are considered. The admittance equations of this circuit are then found, and the values of the equivalent sources I_1' and I_2' are extracted. By the principle of superposition, the values of the equivalent sources needed to account for the effect of the original sources and the initial conditions are then $I_1 + I_1'$ and $I_2 + I_2'$.

To illustrate the several concepts just discussed, the following example is carried through by two methods. The two types of equivalent sources are determined first by the method just discussed, then by considering the sources all at once with a tag (') attached to one type of source to distinguish it from the other type. By adding only tagged quantities to tagged quantities and untagged quantities to untagged quantities during the solution-substitution process, the two types of equivalent sources will be distinguished at the finish. Further, the results of both methods will be identical.

The circuit to be considered is the following:



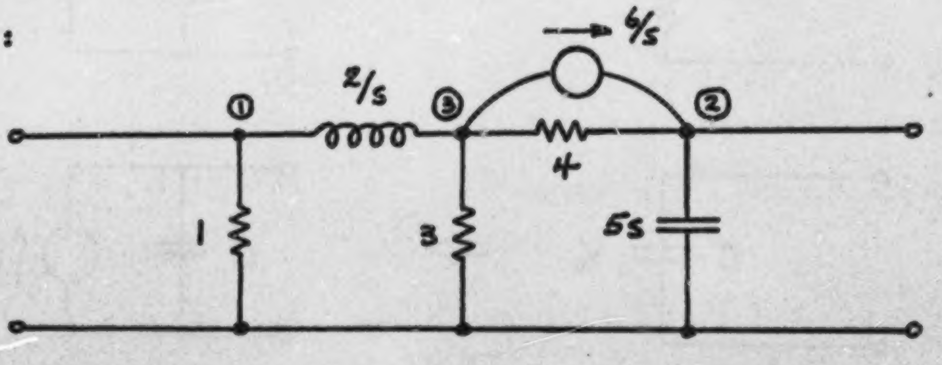
(mhos)

Initial Conditions: $I_o = 7$ amperes

$V_o = 12$ volts

1. Solution by the Principle of Superposition

First the circuit is considered as though all of the initial conditions were zero. The diagram of the circuit which represents this situation is:



For this circuit, the system of equations is found to be:

$$0 = \left(1+\frac{2}{s}\right)E_1 \qquad\qquad \left(-\frac{2}{s}\right)E_3$$

$$\frac{6}{s} = \qquad (5s+4)E_2 + (-4)E_3$$

$$-\frac{6}{s} = \left(-\frac{2}{s}\right)E_1 + (-4)E_2 + \left(7+\frac{2}{s}\right)E_3$$

By eliminating the variable E_3, the admittance equations are determined:

$$\frac{-12}{s\ 7s+2} = \frac{7s+16}{7s+2}E_1 - \frac{8}{7s+2}E_2$$

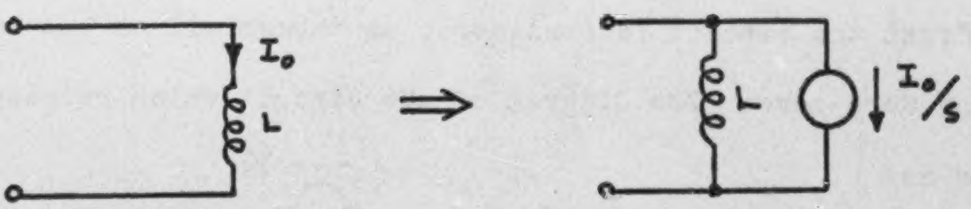
$$\frac{18s+12}{s\ 7s+2} = \frac{-8}{7s+2}E_1 + \frac{35s^2+22s+8}{7s+2}E_2$$

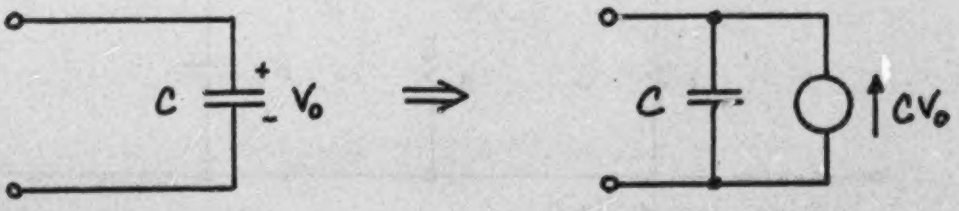
From these equations, it is apparent that the equivalent sources of the first type are:

$$I_1 = \frac{-12}{s(7s+2)}$$

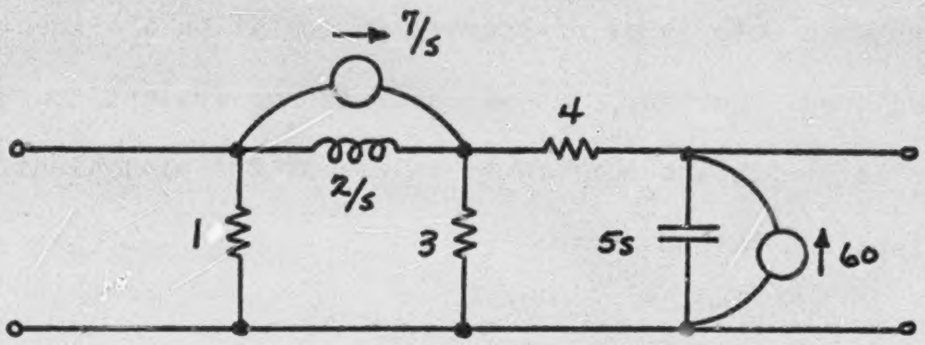
$$I_2 = \frac{18s+12}{s(7s+2)}$$

The first step in finding the equivalent sources of the second type is to transform each element with non-zero initial conditions into its Norton equivalent. That is, the following substitutions are made:





Next, the original source is set to zero (i.e., open-circuited). The diagram is then:



The system of equations is found to be:

$$-\frac{7}{s} = \left(1+\frac{2}{s}\right)E_1 \qquad\qquad + \left(-\frac{2}{s}\right)E_3$$

$$60 = \qquad + (5s+4)E_2 + (-4)E_3$$

$$\frac{7}{s} = \left(-\frac{2}{s}\right)E_1 + (-4)E_2 + \left(7+\frac{2}{s}\right)E_3$$

And thence, by elimination of E_3, the admittance equations:

$$\frac{-49}{7s+2} = \frac{7s+16}{7s+2}E_1 - \frac{8}{7s+2}E_2$$

$$\frac{420s+148}{7s+2} = \frac{-8}{7s+2}E_1 + \frac{35s^2+22s+8}{7s+2}E_2$$

These admittance equations determine the second type of equivalent source:

$$I_1' = \frac{-49}{7s+2}$$

$$I_1' = \frac{420s+148}{7s+2}$$

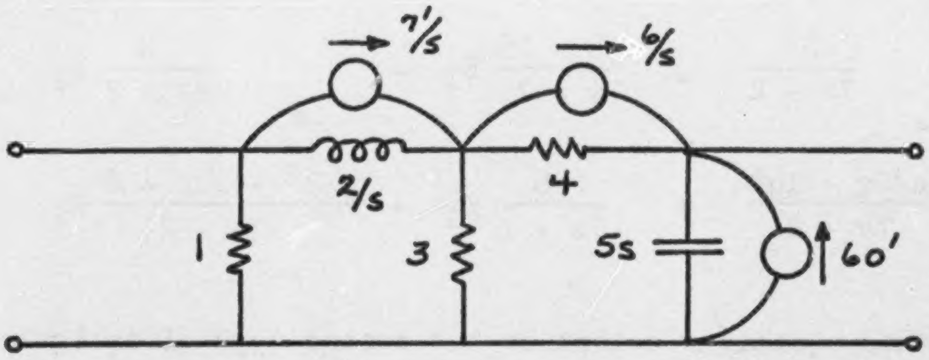
The y_{ik} appearing in the admittance equations, in both cases, are identical. This is reasonable since they are a measure only of the effect of each terminal-pair upon the other terminal-pair, and do not depend upon the sources within the circuit. By the principle of superposition, the y_{ik} of the circuit with both types of sources in operation are identical to the y_{ik} just calculated. Further, the value of the equivalent sources for each terminal-pair is simply the sum of the values of the equivalent sources for each terminal-pair obtained above:

$$I_1 + I_1' = \frac{-49s-12}{s(7s+2)}$$

$$I_2 + I_2' = \frac{420s^2+166s+12}{s(7s+2)}$$

2. Solution by Tags

Alternatively, the circuit is diagrammed below with the value of the original source untagged, and the values of the initial condition sources tagged (by primes):



Below, the equations are presented, where an untagged zero is written to denote that no current is impressed on that node by an original source:

$$0 - \frac{7'}{s} = \left(1 + \frac{2}{s}\right)E_1 + \left(-\frac{2}{s}\right)E_3$$

$$\frac{6}{s} + 60' = + (5s + 4)E_2 + (-4)E_3$$

$$-\frac{6}{s} + \frac{7'}{s} = \left(-\frac{2}{s}\right)E_1 + (-4)E_2 + \left(7 + \frac{2}{s}\right)E_3$$

The dependence of the variable E_3 upon the variables E_1 and E_2 is expressed as:

$$E_3 = \frac{1}{(7 + 2/s)}\left\{\left(\frac{-6}{s} + \frac{7'}{s}\right) + \frac{2}{s}E_1 + 4E_2\right\}$$

This expression, which arose from the third equation, is substituted into the first equation and into the second equation. The two new equations are then put into the proper form, keeping the tagged and untagged quantities separate. The results are:

$$\frac{-12}{s(7s+2)} - \left(\frac{49}{7s+2}\right) = \frac{7s+16}{7s+2}E_1 - \frac{8}{7s+2}E_2$$

$$\frac{18s+12}{s(7s+2)} + \left(\frac{420s+148}{7s+2}\right) = \frac{-8}{7s+2}E_1 + \frac{35s^2+22s+8}{7s+2}E_2$$

As claimed, the results of both methods are identical. They express the algorithm which JOBSHOP uses.

Another Two-port Representation. Since the node-equations discussed up to now are so intimately related to Kirchhoff's current law, it is not difficult to imagine that a similar system of equations might be related to Kirchhoff's voltage law. Such equations do exist, and are known as the loop-equations.[1] The solution-substitution process may be applied to these equations also, producing the impedance equations which are of the form:

$$E_1 + E_1' = z_{11}I_1 + z_{12}I_2$$

$$E_2 + E_2' = z_{21}I_1 + z_{22}I_2$$

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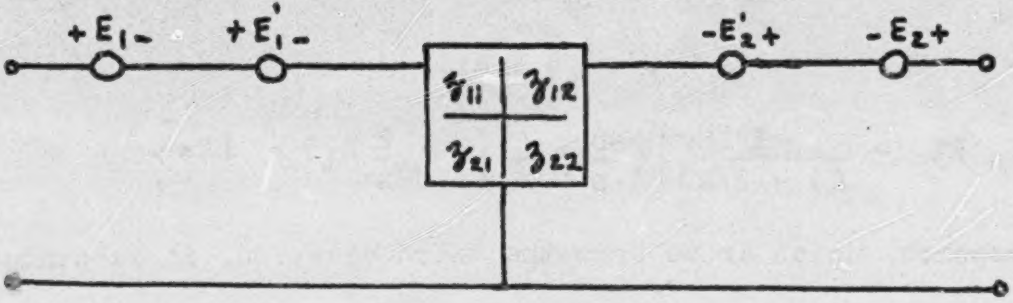
[1] For a discussion of these equations, see an elementary text on circuit theory.

These equations define the Thevinin equivalent two-port:



Unfortunately, it is difficult to write these equations for a circuit which misbehaves topologically. The node-equations, however, can be written without special topological considerations. If only one method is to be used, it is better to determine the admittance equations, and from them, calculate the impedance equations. JOBSHOP follows this procedure.

System Equations Provided By JOBSHOP. Each node-equation is of the form:

$$I_k = g_{k1}E_1 + g_{k2}E_2 + \ldots + g_{kn}E_n$$

where each of the operator-coefficients g_{ik} is of the form:

$$g_{ik} = \frac{1}{s}\left(\frac{1}{L} + Gs + Cs^2\right)$$

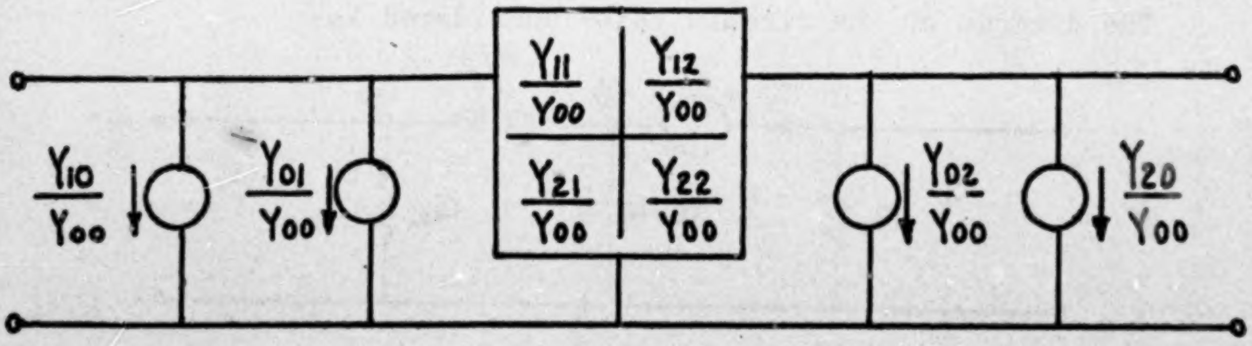
and where s is the complex variable in the frequency-domain representation of the behavior of the circuit. The coefficients g_{ik}, except for the factor $\frac{1}{s}$, are polynomials in s. Since this factor appears in all of the g_{ik}, it may be removed from the original system and then be replaced later in the admittance equations. From this it is easy to see that because the coefficients y_{ik} of the admittance equations will therefore be rational polynomials in s, the solution-substitution process involves only the multiplication and division of the coefficients g_{ik} of the admittance equations. A close examination of the iterative procedure shows that if no common factors are divided out in the solution-substitution process, all of the parameters of the admittance equations will share a common denominator polynomial. The same statement is true for the impedance equations.

If the designer requests, all of the information needed to describe the circuit as an equivalent two-port is printed out. This information is in the form of the admittance representation or in the form of the impedance representation, as desired. In either case, the first polynomial to be printed is the denominator polynomial common to that form of representation; following this polynomial are the numerator polynomials of the equivalent sources and of the various coefficients. The admittance polynomials are labeled with subscripted Y's, and are to be arranged as follows:

$$\frac{Y10}{Y00} + \frac{Y01}{Y00} = \frac{Y11}{Y00} E_1 + \frac{Y12}{Y00} E_2$$

$$\frac{Y20}{Y00} + \frac{Y02}{Y00} = \frac{Y21}{Y00} E_1 + \frac{Y22}{Y00} E_2$$

to define the Norton equivalent two-port:

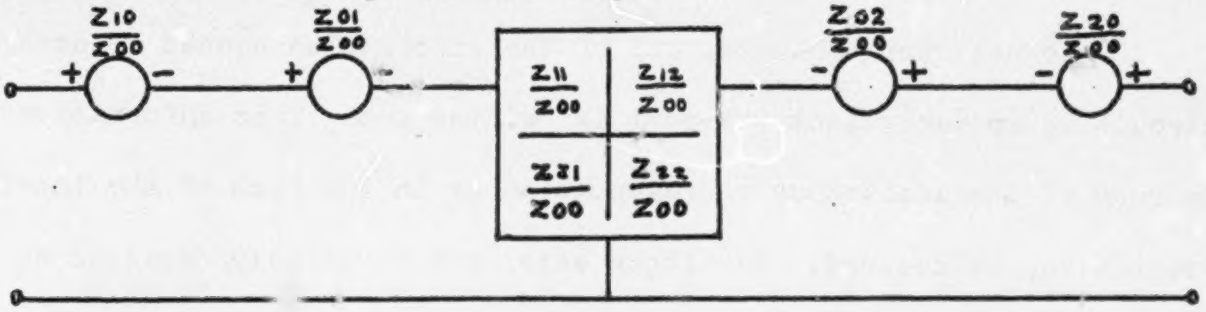


The impedance polynomials are labeled with subscripted Z's, and are to be arranged as follows:

$$\frac{Z10}{Z00} + \frac{Z01}{Z00} = \frac{Z11}{Z00} I_1 + \frac{Z12}{Z00} I_2$$

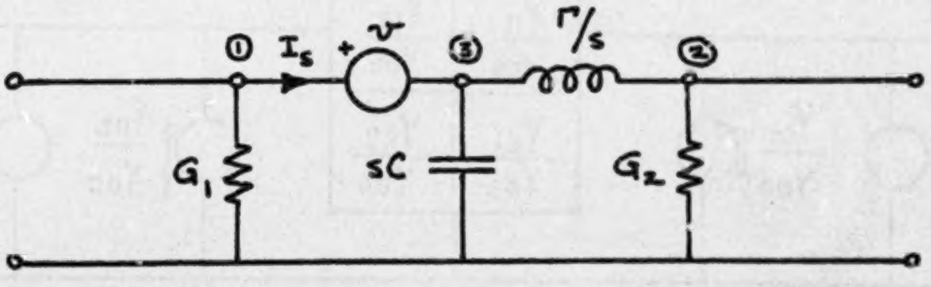
$$\frac{Z20}{Z00} + \frac{Z02}{Z00} = \frac{Z21}{Z00} I_1 + \frac{Z22}{Z00} I_2$$

to define the Thevinin equivalent two-port:



DC Performance. The first 'test' calculations for the circuit yield the constant voltage of each node, and the constant current leaving each node through any attached inductances. For these dc calculations, each inductance is replaced with a short-circuit and each capacitor is replaced with an open circuit. (The assumption is that the constant sources have been in operation so long that all transient current and voltage variations have decayed to zero.) The process of determining these dc operating conditions is illustrated by the following example.

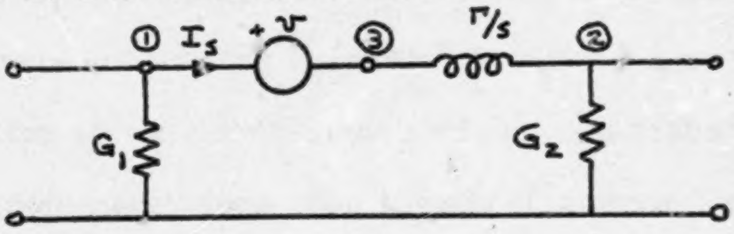
The diagram of the circuit to be considered is:



From this configuration, the node-equations and the equation of constraint introduced by the voltage source are easily found to be:

$$\begin{array}{llllll} I_1 = 0 = & (G_1)\,E_1 & & & + & I_s \\ I_2 = 0 = & & (G_2 + \frac{\Gamma}{s})\,E & - (\frac{\Gamma}{s})\,E_3 & & \\ I_3 = 0 = & & -(\frac{\Gamma}{s})\,E & + (Cs + \frac{\Gamma}{s})\,E_3 & - & I_s \\ V = & E_1 & & - E_3 & & \end{array}$$

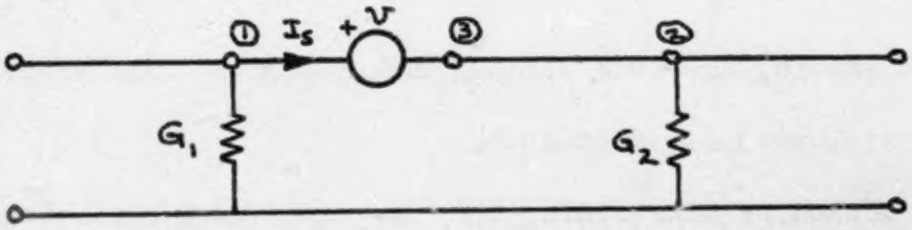
Next the capacitor is removed from the circuit:



This has the effect of setting C = 0, thus altering the equations:

$$\begin{array}{lllll} 0 = & (G_1)\,E_1 & & & + I_s \\ 0 = & & (G_2 + \frac{\Gamma}{s})\,E_2 & - (\frac{\Gamma}{s})\,E_3 & \\ 0 = & & -(\frac{\Gamma}{s})\,E_2 & + (\frac{\Gamma}{s})\,E_3 & - I_s \\ V = & E_1 & & - E_3 & \end{array}$$

Finally, the inductor is replaced with a short-circuit:



This alteration of the configuration has two effects upon the above system of equations:

1. The constraint $E_2 - E_3 = 0$ is introduced since the voltage difference between nodes 2 and 3 has been reduced to zero.
2. The new node, created by the short circuit, has an impressed current $I_2 + I_3$

The equations, when modified in accord to 1 and 2 are:

$$\begin{aligned} 0 &= (G_1)E_1 + I_s \\ 0 &= (G_2)E_2 - I_s \\ V &= E_1 - E_2 \end{aligned}$$

This system of equations has a unique solution for the unknowns E_1, E_2, I_s from which the unknown E_3 may be determined by the equation $E_2 = E_3$. In other words each node-voltage has been determined and also the voltage source current. Since the voltage at each node is known, the current passing through each conductance may be found. Since no dc current may pass through a capacitor, current leaving a node must pass through the conductances, voltage sources, and inductances fastened to that node. Thus, if I_g is the current leaving through conductances, I_s is the current leaving through voltage sources, and I is the current impressed on the node by current sources, thus

$$I' = I - I_g - I_s$$

is the current leaving the node through inductances. This expression for I' is simply evaluated for each node.

This method of determining the dc operating conditions is easily generalized by using matrices. To illustrate, the example is reconsidered.

1) The node-equations are written in matrix notation for the circuit with the voltage source removed

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} G_1 & & \\ & G_2 + \frac{\Gamma}{s} & -\frac{\Gamma}{s} \\ & -\frac{\Gamma}{s} & Cs + \frac{\Gamma}{s} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} .$$

2) The capacitor is replaced with an open-circuit by setting $C = 0$ in the previous matrix

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} G_1 & & \\ & G_2 + \frac{\Gamma}{s} & -\frac{\Gamma}{s} \\ & -\frac{\Gamma}{s} & \frac{\Gamma}{s} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

3) The voltage source introduces the constraint $V = E_1 - E_3$, corresponding to the matrix equation

$$\begin{bmatrix} V \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix}$$

4) Associated with the voltage source is its (unknown) current I_s. This current must be accounted for in the node-equations since the source extracts a current I_s from node 1 and extracts a current $-I_s$ from node 3. This is accounted for by the following composite matrix equation

$$\begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} = \left[\begin{array}{ccc|c} G_1 & & & 1 \\ & G_2+\frac{\Gamma}{s} & -\frac{\Gamma}{s} & 0 \\ & -\frac{\Gamma}{s} & \frac{\Gamma}{s} & -1 \end{array}\right] \left[\begin{array}{c} E_1 \\ E_2 \\ E_3 \\ \hline I_s \end{array}\right]$$

5) The above composite matrix equation is altered again, to include the matrix equation of 3)

$$\left[\begin{array}{c} 0 \\ 0 \\ 0 \\ \hline V \end{array}\right] = \left[\begin{array}{ccc|c} G_1 & & & 1 \\ & G_2+\frac{\Gamma}{s} & -\frac{\Gamma}{s} & 0 \\ & -\frac{\Gamma}{s} & \frac{\Gamma}{s} & -1 \\ \hline 1 & 0 & -1 & 0 \end{array}\right] \left[\begin{array}{c} E_1 \\ E_2 \\ E_3 \\ I_s \end{array}\right]$$

When multiplied out, the resulting system of equations is identical to the system obtained earlier.

In general, the composite matrix equation is of the form

$$\begin{bmatrix} \underline{I} \\ \underline{V} \end{bmatrix} = \begin{bmatrix} \underline{G} & \underline{B}^t \\ \underline{B} & \underline{0} \end{bmatrix} \begin{bmatrix} \underline{E} \\ \underline{I_s} \end{bmatrix}$$

where

$\underline{I}$ is the matrix of impressed currents written for the circuit with the voltage sources removed.

$\underline{V}$ is the matrix of voltage sources.

$\underline{G}$ is the matrix of coefficients of the node-equations written for the circuit with the voltage sources removed.

$\underline{B}$ is the matrix composed of 1's, 0's, -1's, and expresses the constraints introduced by the voltage sources.

$\underline{B}^t$ is the transpose of $\underline{B}$ and expresses the dependence of the impressed currents upon the (unknown) currents pouring through the voltage sources.

$\underline{O}$ is a zero-matrix, and expresses the fact that the voltage of a voltage source is independent of the current passing through it.

$\underline{E}$ is the matrix of (unknown) node-voltages.

$\underline{I}_s$ is the matrix of (unknown) currents pouring through the voltage sources.

Once this composite matrix has been constructed, the capacitors must be removed from the circuit. This is accomplished by setting the coefficients of s to zero in the composite matrix.

The substitution of short-circuits for inductors is accomplished by means of matrix algebra. There is a matrix $\underline{A}$ constructed to relate the node-voltages and voltage-source currents to a new set of node-voltages and voltage-source currents. The new set of independent voltages and currents arise from the fact that the voltages between which an inductor is fastened are no longer independent (distinct). The matrix $\underline{A}$ is constructed from the goemetry of the circuit, its entries being determined by the locations of the inductors within the circuit. The equation relating the old basis to the new basis is

$$\begin{vmatrix} \underline{E} \\ \underline{I}_s \end{vmatrix} = \underline{A} \begin{vmatrix} \underline{E}' \\ \underline{I}_s' \end{vmatrix}$$

Upon substituting this expression into the composite matrix equation, the result is

$$\begin{vmatrix} \underline{I} \\ \underline{Y} \end{vmatrix} = \begin{vmatrix} \underline{G} & \underline{B}^t \\ \underline{B} & \underline{0} \end{vmatrix} \underline{A} \begin{vmatrix} \underline{E}' \\ \underline{I}_s' \end{vmatrix}$$

However, since nodes between which an inductance is fastened are joined by a short-circuit, the new node has an impressed current equal to the sum of the currents impressed upon the two separate nodes. It can show that the following matrix multiplication affects this addition of currents

$$\begin{vmatrix} \underline{I}' \\ \underline{Y}' \end{vmatrix} = \underline{A}^t \begin{vmatrix} \underline{I} \\ \underline{Y} \end{vmatrix}$$

That is the entries of $\begin{vmatrix} \underline{E}' \\ \underline{I}_s' \end{vmatrix}$ may be found from the equation

$$\begin{vmatrix} \underline{I}' \\ \underline{Y}' \end{vmatrix} = \underline{A}^t \begin{vmatrix} \underline{G} & \underline{B}^t \\ \underline{B} & \underline{0} \end{vmatrix} \underline{A} \begin{vmatrix} \underline{E}' \\ \underline{I}_s' \end{vmatrix}$$

where

$$\begin{vmatrix} \underline{I}' \\ \underline{Y}' \end{vmatrix} = \underline{A}^t \begin{vmatrix} \underline{I} \\ \underline{Y} \end{vmatrix}$$

After the new basis voltage and currents have been determined by the solution of simultaneous equations, the original node-voltages and source currents may be found from the equations of constraint introduced by the appearance of inductances. This stems directly from the equations $E_i - E_j$ where i and j are nodes connected by an inductance. From this information, the current leaving through inductances may be found as described earlier.

When requested, the values of the node-voltages are used also to compute the dc operating conditions of each circuit element. That is, the terminal-pair voltages and the terminal currents are computed from the node-voltages of the complete circuit. This information allows the designer to see immediately whether elements such as transistors or vacuum tubes are properly biased. Also at this stage, the rating of each element is computed on the basis of its operating conditions. For resistive and conductive elements the rating is in power units, for capacitive elements the rating is in voltage units, and for inductive elements the rating is in current units.

Dynamic Performance. Only the test for dc operating conditions is performed upon the original node-equations. The two other tests are performed upon the two-port admittance- or impedance-equations. The first of these tests involves the calculation of the response of the circuit at specified frequencies. These calculations are made by evaluating the system functions, which are the parameters of the two-port equations or certain of their ratios.[1]

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[1] The ratios arise from the admittance equations (or impedance equations) by taking voltage ratios (or current ratios) under various terminal conditions. For example the voltage ratio:

$$A_{21} = \frac{E_2}{E_1} = -\frac{Y_{21}}{Y_{22}}$$

arises from the admittance equation:

$$I_2 = \frac{Y21}{Y00} E_1 + \frac{Y22}{Y00} E_2$$

under the terminal condition $I_2 = 0$. (i.e., the output terminals are open-circuited.) Section I.B should be consulted for the complete list of available ratios.

The system functions are rational polynomials in s and are evaluated under the substitution $s = j\omega$, where ω is the angular frequency specified by the designer. The result is a complex number $a + jb$ is converted into polar coordinates, $M\angle\theta$, and the magnitude M is converted into the gain, $G = 20\log_{10}(M)$, (in db.) The three measures of response $a + jb$, $M\angle\theta$, G are printed in tabular form or are graphed as functions of the frequency ω.

The second of the dynamic tests involves the calculation of the natural frequencies of the circuit. These frequencies correspond to the poles and zeros of the system functions. The zeros of the system function correspond to the roots of its numerator polynomial, and the poles correspond to the roots of the denominator polynomial. The roots are determined by a combination of Bairstow's and Newton's methods.

These tests are closely related: if the frequency response of the circuit is known, the polynomial ratio which best fits the response curve may be found and the poles and zeros of this ratio may then be determined. Likewise, if the poles and zeros are known, the polynomial ratio which they represent may be constructed and evaluated at specified frequencies. Both forms of tests are provided since conversion from one form to the other is extremely tedious. In any case, it should be recalled that the two-port equations represent the original circuit, and are merely a short-hand method of specifying lengthy lists of response data.

From any Circuit to Node-equations. Because JOBSHOP is a computer program, it must have a standard method for accomplishing each of its operations. The fundamental operation of establishing the node-equations is no exception: the equations must be created by a method which is effective for all circuits. The following few paragraphs describe such a method. It is distinct from the method used in the examples, but both methods yield the same system of equations.

For every node k of any linear circuit, an equation of the form:

$$I_k = g_{k1}E_1 + g_{k2}E_2 + \dots + g_{kn}E_n$$

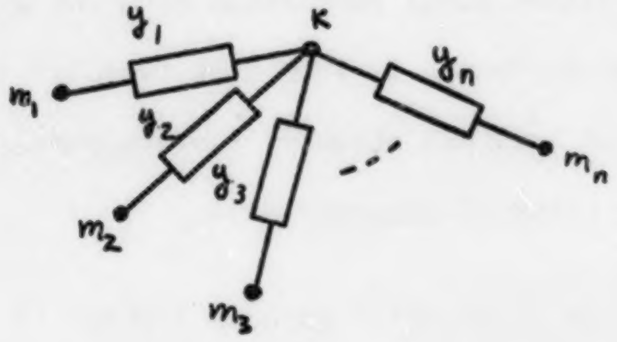
may be written to express the linear dependence of the current I_k impressed on node k to the node-voltages (E_m). The coefficients g_{km} depend upon the circuit under consideration; that is, they arise from the arrangement and value of the components within the circuit.

If the node k has fastened to it only two-terminal inductance-, conductance-, and capacitance-elements, then the g_{km} are defined as follows

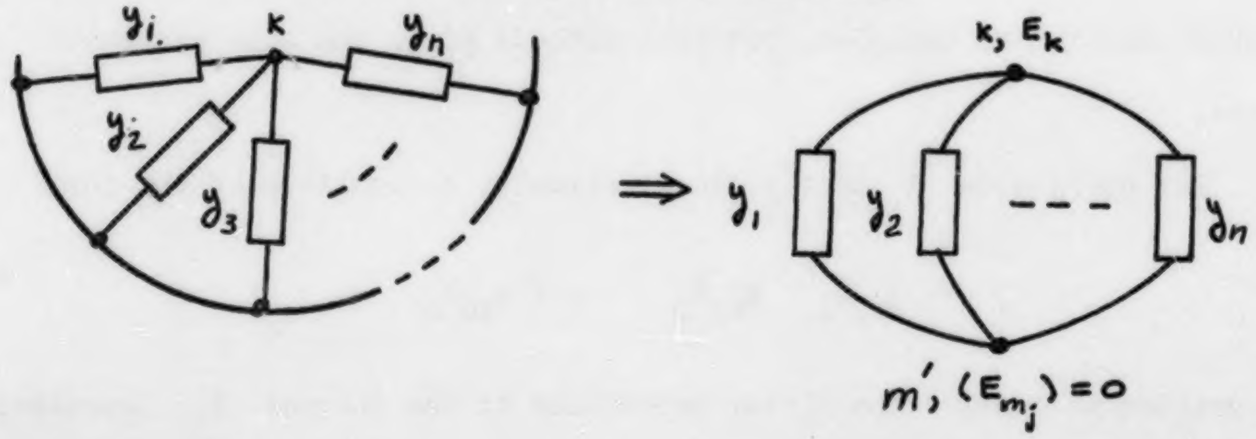
g_{kk} = the sum of the admittances attached to node k

$-g_{km}$ $(k \neq m)$ = the sum of the admittances which connect nodes m and k.

Verification of g_{kk}. Let the circuitry at node k be as diagrammed:



where the m_j are all of the nodes of the circuit other than node k, and y_j is the total admittance connecting nodes m_j and k. All of the nodes, except node k, are connected by an ideal conductor:



The connected nodes (m_j) form a new node m', and the node-voltages (E_{m_j}) are all zero; hence, from the node-equation

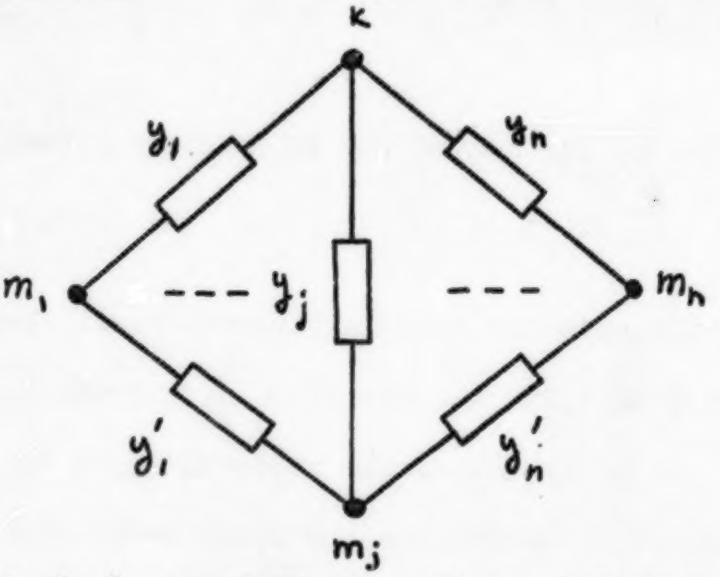
$$I_k = g_{kk}E_k \quad \text{or} \quad g_{kk} = \frac{I_k}{E_k}$$

The ratio $\frac{I_k}{E_k}$ is the total admittance between the new node m' and the node k; that is

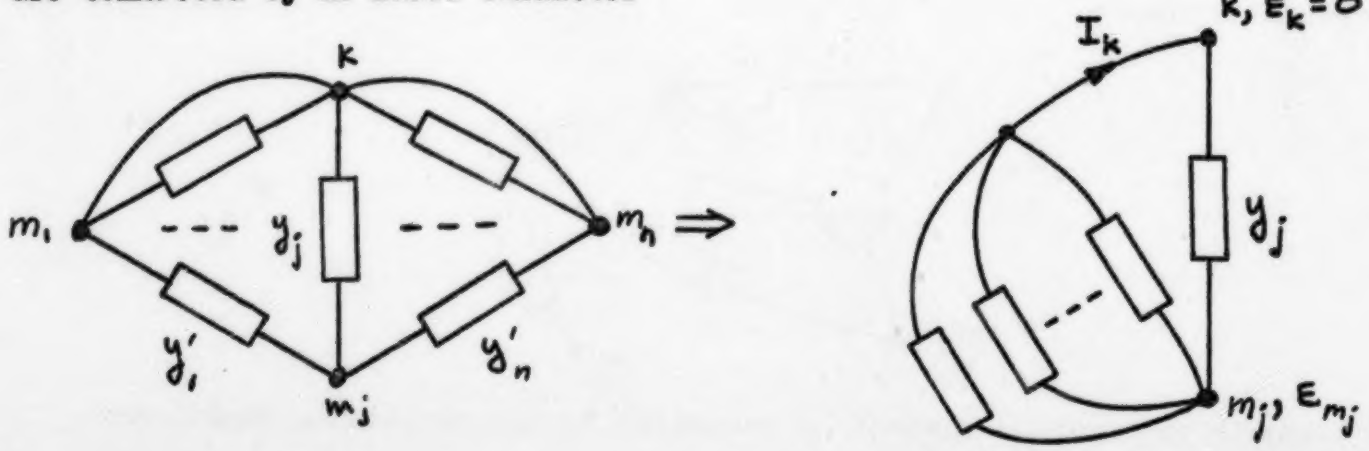
$$g_{kk} = \frac{I_k}{E_k} = \sum_{j=1}^{n} y_{m_j} ,$$

as claimed.

Verification of g_{km} $(k \neq m)$. Let the circuitry at nodes k and m_j be as diagrammed:



where the (m_j) and (y_j) are defined as above, and where y'_p is the total admittance between nodes m_j and $m_p (p \neq j)$. All of the nodes, except m_j are connected by an ideal conductor



The current flowing from node m_j to node k through the admittance y_j is $y_j E_{m_j}$. Since there are no other current paths, the current I_k impressed on node k by the ideal conductor is $-y_j E_{m_j}$; that is

$$I_k = -y_j E_{m_j}, \quad \text{or} \quad \frac{I_k}{E_{m_j}} = y_j$$

Because the only non-zero voltage is E_{m_j}, the node-equation states

$$I_k = g_{km_j} E_{m_j} \quad \text{or} \quad g_{km_j} = \frac{I_k}{E_{m_j}}$$

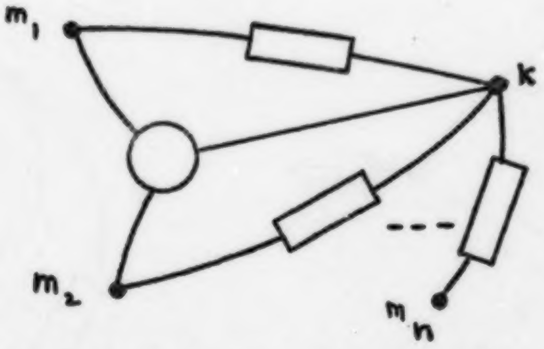
Therefore

$$g_{km_j} = -y_{m_j}$$

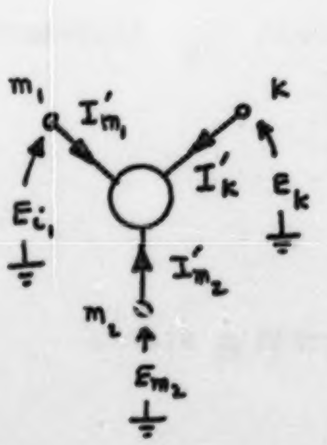
which is, by definition, the sum of the admittances between nodes k and m_j.

Extension of g_{km}. Circuits may contain three-terminal elements such as transistors or tubes; in this case the above definition of the g_{km} is meaningless if k or m is one of the nodes to which the element is fastened. It is necessary to generalize the above definition.

Let the following be the diagram of a circuit containing a three-terminal element fastened to node k, the rest of the components being two-terminal elements:



Let the three-terminal element be described by the admittance equations:

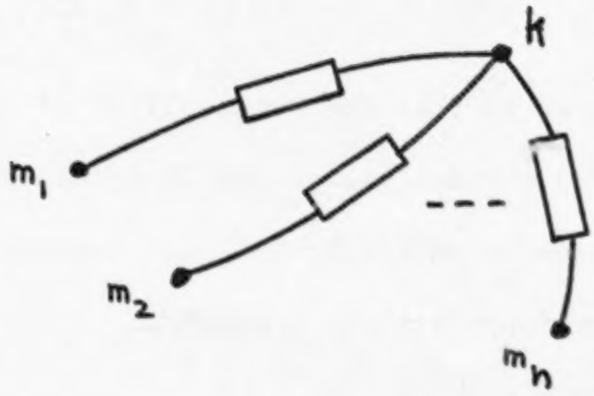


$$I'_k = y_{kk} E_k + y_{km_1} E_{m_1} + y_{km_2} E_{m_2}$$

$$I'_{m_1} = y_{m_1k} E_k + y_{m_1m_1} E_{m_1} + y_{m_1m_2} E_{m_2}$$

$$I'_{m_2} = y_{m_2k} E_k + y_{m_2m_1} E_{m_1} + y_{m_2m_2} E_{m_2}$$

The three-terminal element is removed from the circuit, leaving the remaining circuit as diagrammed:



For this new circuit, the node-equation for node k may be established, using the previous definitions of the g_{km} since the circuit now contains only two-terminal elements

$$I_k = g_{kk}E_k + g_{km_1}E_{m_1} + g_{km_2}E_{m_2} + g_{km_3}E_{m_3} + \dots + g_{km_n}E_{m_n}$$

The expression on the right represents the current extracted from node k by the two-terminal elements fastened to it; the expression

$$y_{kk}E_k + y_{km_1}E_{m_1} + Y_{km_2}E_{m_2}$$

represents the current extracted from node k by the three-terminal element; hence, the total current extracted from node k by all of the elements is simply the sum of these expressions, and the result must equal the impressed current I_k:

$$\begin{aligned} I_k &= g_{kk}E_k + g_{km_1}E_{m_1} + g_{km_2}E_{m_2} + \dots + g_{km_n}E_{m_n} + \\ &\quad y_{kk}E_k + y_{km_1}E_{m_1} + y_{km_2}E_{m_2} \\ &= (g_{kk} + y_{kk})E_k + (g_{km_1} + y_{km_1})E_{m_1} + (g_{km_2} + y_{km_2})E_{m_2} + \dots \\ &\quad - g_{km_n}E_{m_n} \end{aligned}$$

By this same method, the total node-equation for the nodes m_1 and m_2 may be established.

The important result here is that the total effect of an element may be accounted for by simply adding its admittance coefficients y_{km} to the node-equations g_{km}. This process is valid for the two-terminal elements already considered, and also for four-terminal elements.

Matrix Notation. Associated with a circuit of $n+1$ nodes, there are always n equations expressing the current at the nodes in terms of the n independent node-voltages. It is convenient to think of this system of equations as one matrix equation:

$$\underline{I,I'}\rangle = \underline{G}\ \underline{E}\rangle$$

where the entries of the matrices are defined by the parameters of the node-equations:

$$\begin{bmatrix} I_1, I'_1 \\ I_2, I'_2 \\ \vdots \\ I_n, I'_n \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & \cdots & g_{1n} \\ g_{21} & g_{22} & \cdots & g_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ g_{n1} & g_{n2} & \cdots & g_{nn} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ \vdots \\ E_n \end{bmatrix}$$

The peculiar notation $\underline{I,I'}\rangle$ is used to indicate that the current sources and the initial-condition sources are kept separate throughout the calculations.

For a two-, three-, or four-terminal component, a similar matrix equation: $\underline{I,I'}\rangle_y = \underline{Y}\ \underline{E}\rangle$ may be written to express its admittance equations. The matrices for a three-terminal component fastened to nodes m_1, m_2, m_3 are defined as follows:

$$\begin{vmatrix} I_{m_1}, I'_{m_1} \\ I_{m_2}, I'_{m_2} \\ I_{m_3}, I'_{m_3} \end{vmatrix} = \begin{vmatrix} y_{m_1m_1} & y_{m_1m_2} & y_{m_1m_3} \\ y_{m_2m_1} & y_{m_2m_2} & y_{m_2m_3} \\ y_{m_3m_1} & y_{m_3m_2} & y_{m_3m_3} \end{vmatrix} \begin{vmatrix} E_{i_1} \\ E_{i_2} \\ E_{i_3} \end{vmatrix}$$

Finally, a matrix-operation $\oplus$ is defined (here for $\underline{Y}$ representing the matrix of a three-terminal element) as follows

$$G = \underline{G} \oplus \underline{Y}$$

where

$$g'_{ik} = \begin{cases} g_{mk} - y_{mk} & \text{if} \quad \begin{matrix} i = (m_1 \text{ or } m_2 \text{ or } m_3) \text{ and} \\ k = (m_1 \text{ or } m_2 \text{ or } m_3) \end{matrix} \\ g_{mk} & \text{otherwise} \end{cases}$$

The definition of the $\oplus$-operation is merely a formal statement of the fact that the total effect of an element may be accounted for by adding its admittance coefficients to the admittance coefficients of the node-equations of the circuit with the element removed. The resulting matrix $\underline{G'}$ is then the matrix which represents the behavior of the total circuit, by means of the matrix equation

$$\underline{I,I'}\rangle = \underline{G'}\underline{E}\rangle$$

Since the new matrix $\underline{G'}$ replaces the old matrix $\underline{G}$, it is consistent to write

$$\underline{G} = \underline{G} \oplus \underline{y}$$

when it is meant that

$$\underline{G} \oplus \underline{y} \longrightarrow \underline{G}$$

The operation can be extended to include the operation

$$\underline{I,I'}\rangle = \underline{I,I'}\rangle \oplus \underline{I,I'}\rangle_y$$

From repeated application of the $\oplus$-operation, the matrix equation

$$\underline{I,I'}\rangle = \underline{G}\ \underline{E}\rangle$$

is constructed from a list of the components in the circuit.

Logic of Execution. The designer specifies his circuit to JOBSHOP by means of punched data cards. Each data card contains all of the information needed to completely determine the behavior of the component which that data card represents; that is, the data card identifies the nodes to which the component is to be attached, the parameters of the component, and a mnemonic symbol indicating 'how' the parameters describe the component. From these data cards, the matrix equation for the complete circuit is written by the following iterative steps.

1. The matrix $\underline{G}$ is initially set to zero, indicating that the circuit has, at present, no elements.

2. A data card is 'read' and its contents are examined to see if the card represents a component. If the check indicates that the card does not represent a component, then the list of components has been exhausted, so that the equation $\underline{I,I'}\rangle = \underline{G}\ \underline{E}\rangle$ has been written, and the procedure is ended. Otherwise the following steps are performed:

3. The mnemonic symbol is checked. If the symbol indicates that

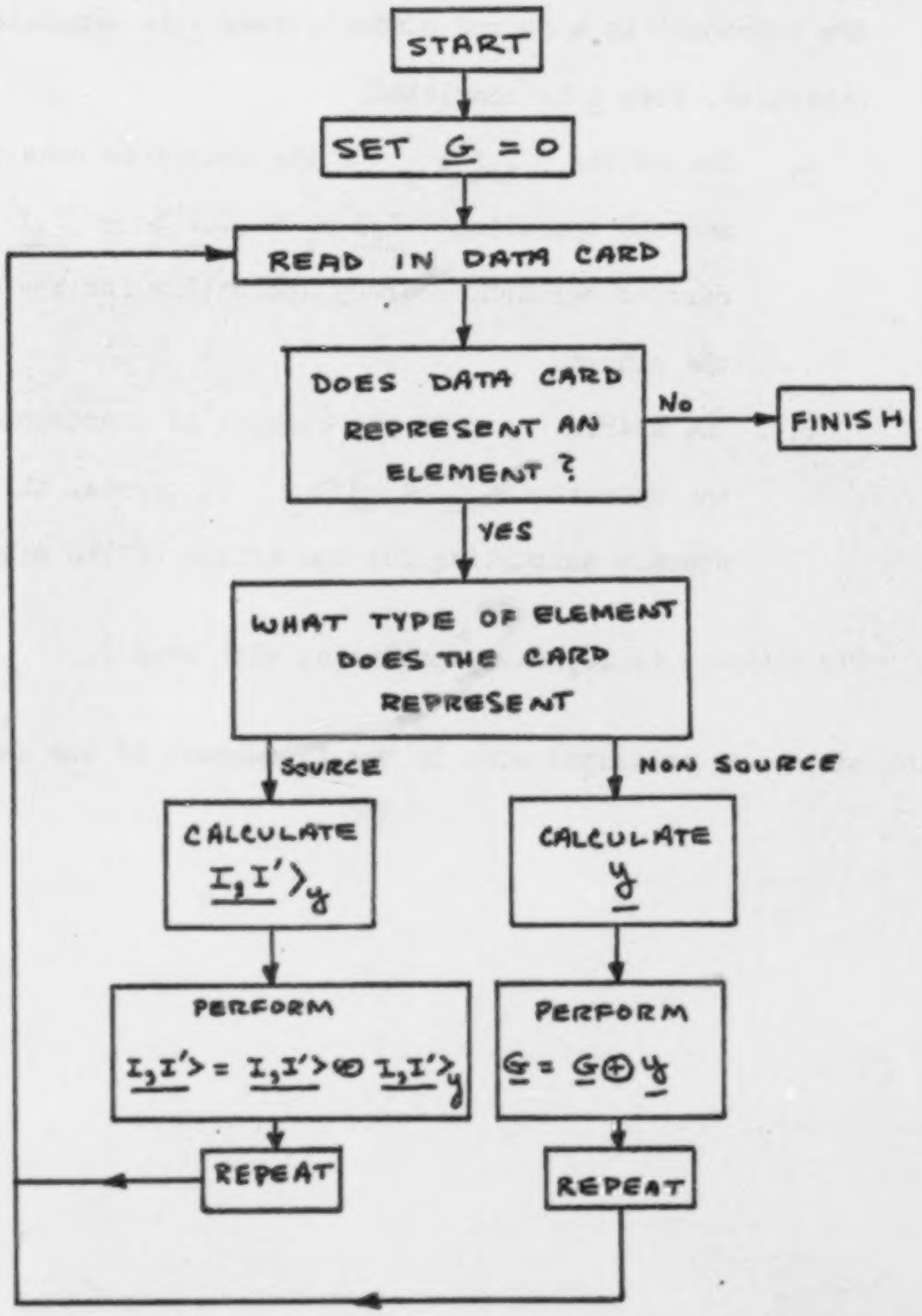
the component is a source element, step *a* is completed; otherwise, step *b* is completed.

a. The matrix $\underline{I,I'}>_y$ of the source is constructed, and the operation $\underline{I,I'}> = \underline{I,I'}> \oplus \underline{I,I'}>_y$ is carried through, thereby accounting for the effect of the source.

b. The matrix $\underline{y}$ of the element is constructed, and the operation $\underline{G} = \underline{G} \oplus \underline{y}$ is carried through, thereby accounting for the effect of the element.

4. The process is repeated, beginning with step 2.

The foregoing steps are presented also in the flow-chart of the following page.


START
SET G = 0
READ IN DATA CARD
DOES DATA CARD REPRESENT AN ELEMENT ?
NO
FINISH
YES
WHAT TYPE OF ELEMENT DOES THE CARD REPRESENT
SOURCE
NON SOURCE
CALCULATE
$\underline{I}, \underline{I'}\rangle_y$
CALCULATE
$\underline{y}$
PERFORM
$\underline{I}, \underline{I'}\rangle = \underline{I}, \underline{I'}\rangle \otimes \underline{I}, \underline{I'}\rangle_y$
PERFORM
$\underline{G} = \underline{G} \oplus \underline{y}$
REPEAT
REPEAT

Elements. The following sections deal with the elements which may be used in circuits to be investigated by JOBSHOP. Presented are the mnemonic which indicates the nature of the element, the equations which describe the behavior of the element, and its associated $\underline{y}$ -matrix or $\underline{I,I'}\rangle_{\underline{y}}$ -matrix. Whenever possible, the elements will be introduced in classes.

Simple Elements. The resistance, inductance, capacitance, conductance, and hybrid-conductance elements (mnemonics R, L, C, G, and H) are considered to be two-port devices. Each type has its own distinct set of definitive equations, but let it suffice that their behavior may also be described by a set of admittance equations

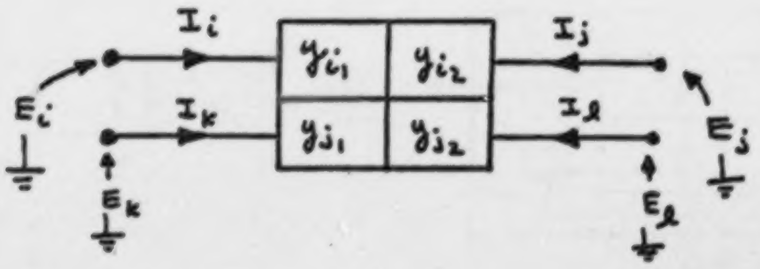
$$I_i = Y_{i_1}(E_i - E_k) + Y_{i_2}(E_j - E_e)$$

$$I_j = Y_{j_1}(E_i - E_k) + Y_{j_2}(E_j - E_e)$$

$$I_k = -I_i$$

$$I_\ell = -I_j$$

This device is represented by the following symbol



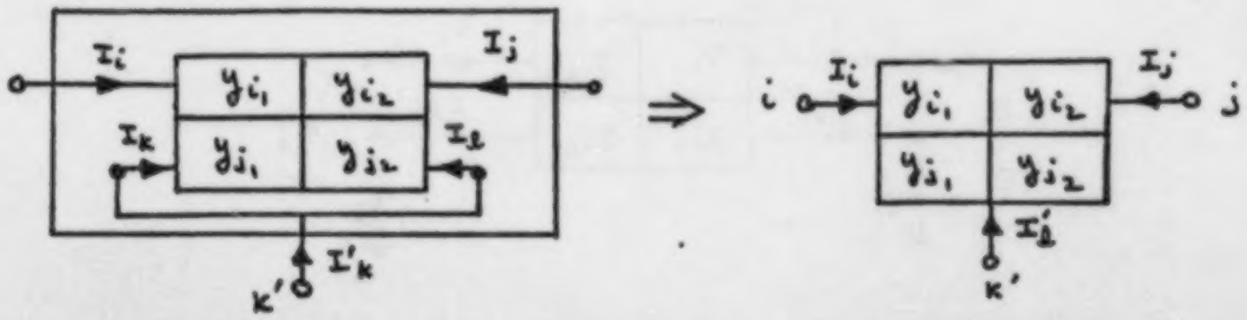
which serves to define the I's and the E's of the preceding equations. (Note that the usual constraint on two-ports is in effect here: the primary terminals are isolated from the secondary terminals; that is, the current entering the two-port through one primary terminal must leave the two-port through the other primary terminal; a similar statement is valid for the secondary terminal-pair.) The element is assumed to be sourceless (i.e., passive), so that its $\underline{I,I'}>_y$-matrix has zero entries everywhere. The y -matrix, however, is found directly from the equations

$$\underline{y} = \begin{bmatrix} y_{i_1} & y_{i_2} & -y_{i_1} & -y_{i_2} \\ y_{j_1} & y_{j_2} & -y_{j_1} & -y_{j_2} \\ -y_{i_1} & -y_{i_2} & y_{i_1} & y_{i_2} \\ -y_{j_1} & -y_{j_2} & y_{j_1} & y_{j_2} \end{bmatrix}$$

If the designer has specified that the element has four terminals, then the operation

$$\underline{G} = \underline{G} \oplus \underline{y}$$

is performed, thus accounting completely for the effect of the element. Otherwise, it is assumed that the terminals k and m have been joined by an ideal conductor; that is, the device has been transformed into a three-terminal device



With the terminals joined in this manner, it is apparent that

$$E_{k'} = E_k = E_1 \quad \text{and}$$

$$I'_k = I_k + E_\ell$$

These two equations, in combination with the previous admittance equations, produce the new admittance equations for the altered element

$$I_i = y_{i_1}E_1 + y_{i_2}E_2 - (y_{i_1} + y_{i_2})E_{k'}$$

$$I_j = y_{j_1}E_i + y_{j_2}E_2 - (y_{j_1} + y_{j_2})E_{k'}$$

$$I_{k'} = -(y_{i_1} + y_{j_1})E_i - (y_{i2} + y_{j_2})E_2 +$$

$$(y_{i_1} + y_{i_2} + y_{j_1} + y_{j_2})E_{k'}$$

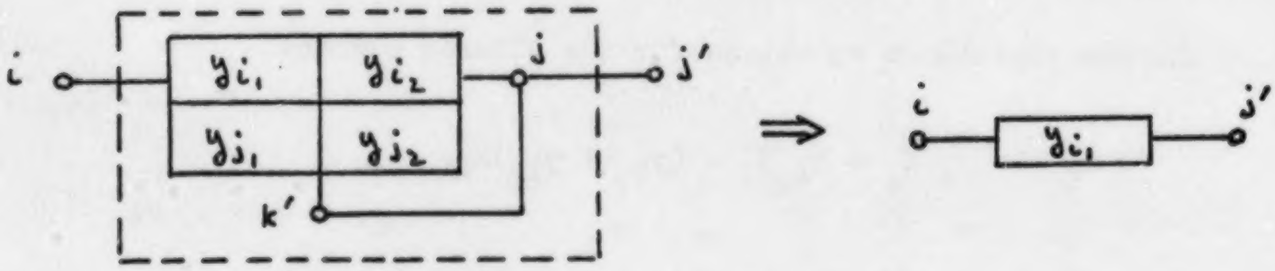
These new admittance equations imply a new $\underline{y}$ -matrix, which is again found directly from the equations

$$\underline{y} = \begin{bmatrix} y_{i_1} & y_{i_2} & -(y_{i_1} \oplus y_{i_2}) \\ y_{j_1} & y_{j2} & -(y_{j_1} \oplus y_{j2}) \\ -(y_{i_1} + y_{j_1}) & -(y_{i_2} + y_{j_2}) & (y_{i_1} + y_{i_2} \oplus y_{j_1} + y_{j_2}) \end{bmatrix}$$

If the designer has indicated that the element has three terminals, then the operation

$$\underline{G} = \underline{G} \oplus \underline{y}$$

is performed, using the $\underline{y}$ -matrix just mentioned. The effect of the element is thereby accounted for. Otherwise, it is assumed that an ideal conductor joins the terminals at nodes k' and j; again the element is transformed.



The connecting of the two terminals introduces more equations of constraint

$$E_{j'} = E_{k'} = E_j$$

$$I_{j'} = I_j + I_{k'}$$

These equations, in combination with the previous equations, yield the new admittance equations

$$I_i = y_{i_1}E_i - y_{i_1}E_{j'}$$

$$I_{j'} = -y_{i_1}E_i + y_{i_1}E_{j'}$$

And from these equations, a new $\underline{y}$ -matrix arises

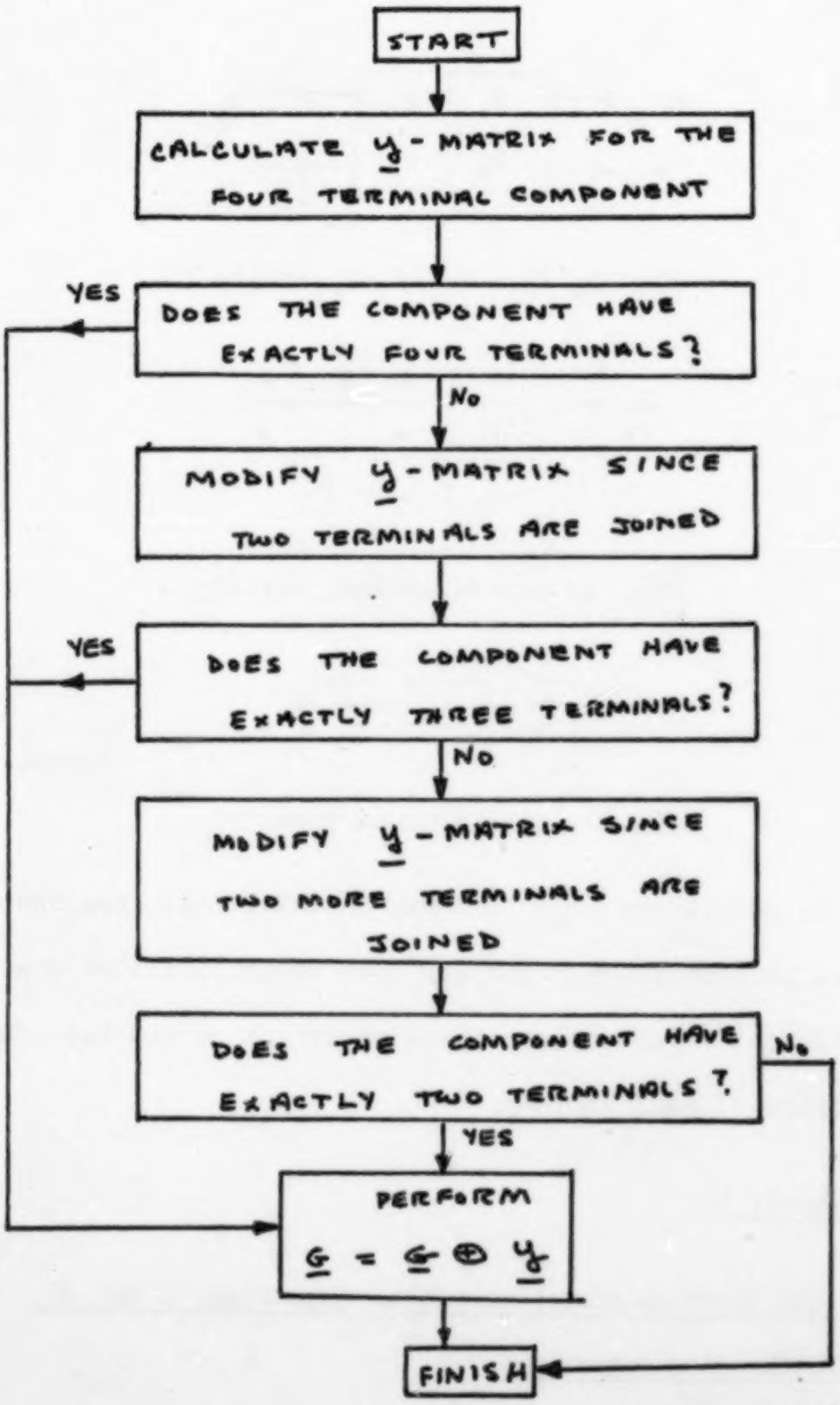
$$\underline{y} = \begin{vmatrix} y_{i_1} & -y_{i_1} \\ -y_{i_1} & y_i \end{vmatrix}$$

Since there are no one terminal elements, this last $\underline{y}$ -matrix is used to alter the $\underline{G}$ -matrix

$$\underline{G} = \underline{G} \oplus \underline{y}$$

and therefore account for the effect of the element.

The following flow-chart represents thes steps.


START
CALCULATE $\underline{y}$ - MATRIX FOR THE FOUR TERMINAL COMPONENT
DOES THE COMPONENT HAVE EXACTLY FOUR TERMINALS?
YES
NO
MODIFY $\underline{y}$ - MATRIX SINCE TWO TERMINALS ARE JOINED
DOES THE COMPONENT HAVE EXACTLY THREE TERMINALS?
YES
NO
MODIFY $\underline{y}$ - MATRIX SINCE TWO MORE TERMINALS ARE JOINED
DOES THE COMPONENT HAVE EXACTLY TWO TERMINALS?
NO
YES
PERFORM $\underline{G} = \underline{G} \oplus \underline{y}$
FINISH

Because the simple elements are so similar, the diagrams which represent these elements are presented below and shall be referred to in the ensuing descriptions.

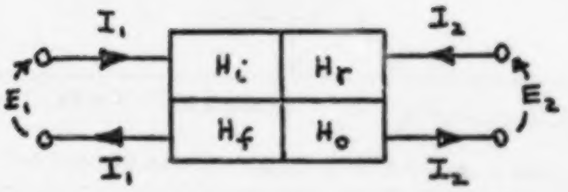


Fig. 1, four-terminal variety.

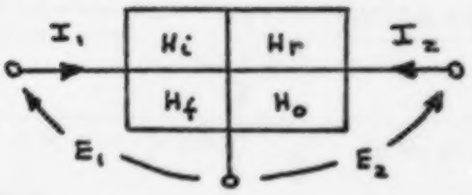


Fig. 2, three-terminal variety.

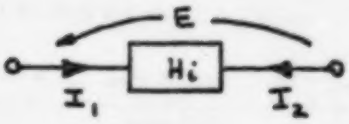


Fig. 3, two-terminal variety.

In order that the admittance equations may be determined from the definitive equations, it is in some cases necessary that restrictions be placed on the values of the element's parameters; these restrictions are included below, with the discussion of each variety.

Resistance (Mnemonic R).

Four- and three-terminal varieties (see Figs. 1 and 2)

Definitive equations

$$E_1 = H_i I_1 + H_r I_2$$

$$E_2 = H_f I_1 + H_o I_2$$

Restrictions

$$(H_i)(H_o) - (H_f)(H_r) \neq 0$$

Two-terminal variety (see Fig. 3)

Definitive equations

$$E = H_i I_1$$

$$E = -H_i I_2$$

Restrictions

$$H_i \neq 0$$

Inductance (Mnemonic L).

Four- and three-terminal varieties (see Figs. 1 and 2)

Definitive equations

$$E_1 = (sH_i)I_1 + (sH_r)I_2$$

$$E_2 = (sH_f)I_1 + (sH_o)I_2$$

Restrictions

$$(H_i)(H_o) - (H_f)(H_r) \neq 0$$

Two-terminal variety (see Fig. 3)

Definitive equations

$$E = (sH_i)I_1 \quad , \quad E = -(sH_i)I_2$$

Restrictions

$$H_i \neq 0$$

Capacitance (Mnemonic C).

Four- and three-terminal varieties (see Figs. 1 and 2)

Definitive equations

$$I_1 = (sH_i)E_1 + (sH_r)E_2$$

$$I_2 = (sH_f)E_1 + (sH_o)E_2$$

Restrictions

None

Two-terminal variety (see Fig. 3)

Definitive equations

$$I_1 = (sH_i)E \quad , \quad I_2 = -(sH_i)E$$

Restrictions

None

Conductance (mnemonic G).

Four- and three-terminal varieties (see Figs. 1 and 2)

Definitive equations

$$I_1 = H_iE_1 - H_rE_2$$

$$I_2 = H_fE_1 - H_oE_2$$

Restrictions

None

Two-terminal variety (see Fig. 3)

Definitive equations

$$I_1 = H_iE \quad , \quad I_2 = -H_iE$$

Restrictions

None

Hybrid-Conductance (Mnemonic H).

Four- and three-terminal varieties (see Figs. 1 and 2)

Definitive equations

$$E_1 = H_i I_1 + H_r E_2$$

$$I_2 = H_f I_1 + H_o E_2$$

Restrictions

$$H_i \neq 0$$

Two-terminal variety (see Fig. 3)

Definitive equations

$$E = H_i I_1 \quad , \quad E = -H_i I_2$$

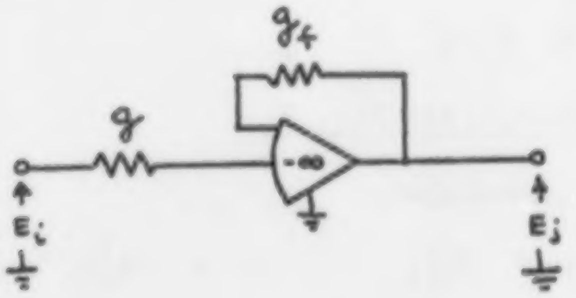
Restrictions

$$H_i \neq 0$$

Operational Amplifier Elements. To provide a greater range in JOBSHOP's capabilities, the operational amplifier elements and the unistor element have been added to the list of available components. These elements are ideal and could not have been simulated using only the previously described elements. Each of these elements is a three-terminal device consisting of an input, an output, and a ground terminal; *it is automatically assumed that the common terminal is fastened to the ground node of the circuit.*

Since the operational amplifier elements are ideal, there may be fastened to a node the output of only one of these elements, for if the outputs of two amplifiers were fastened to the same node, the voltage at that node would, in general, be required to have distinct values simultaneously - an inconsistent requirement!

The voltage at the output of an ideal operational amplifier depends only upon thevoltages at its various input nodes and in no way upon the circuit load fastened to the output node. The present equation written for the output node is evidently no longer valid, and must be replaced. For example, the scalor element consists of an operational amplifier of infinite negative amplification in combination with one feedback conductance g_f and an input conductance g



The equation relating the output voltage E_j to the input voltage E_i is then

$$E_j = \frac{-g}{g_f} E_i \quad \text{or}$$

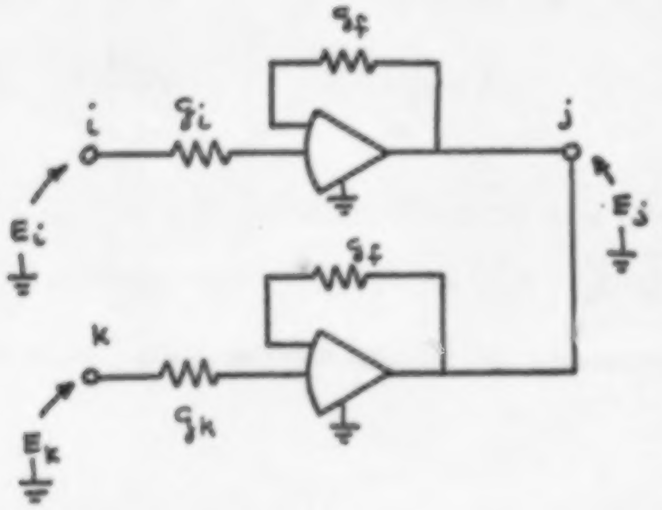
$$0 = -g_f E_j - g E_i$$

This equation, being of the proper form, is used to replace the old, invalidated equation. The $\underline{y}$-matrix describing this element is

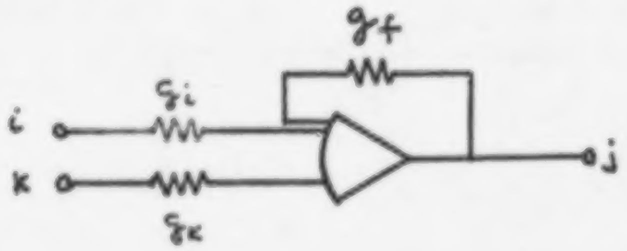
$$\underline{y} = \begin{vmatrix} g & 0 \\ -g & -g_f \end{vmatrix}$$

However, before the operation $\underline{G} = \underline{G} \oplus \underline{y}$ is performed, the entire j-th row (the row corresponding to the output node of the scalor) of the equation $\underline{I,I'}\rangle = \underline{G}\ \underline{E}\rangle$ is set to zero.

If the scalor with output at node j is to have two inputs, one from node i and one from node k, the designer specifies that two scalors, one with input at node i and one with input at node k, are to be fastened to node j



Since this configuration is inconsistent in its requirements on the output voltage E_j, the *configuration is automatically interpreted as signifying one scalor with two inputs*



The two scalors specified by the designer must have the same value of feedback conductance. The equation representing the scalor with feedback conductances g_f and input conductances g_i and g_k is

$$E_j = \frac{-g_i}{g_f} E_i - \frac{g_k}{g_f} E_k \quad \text{or}$$

$$0 = -g_f E_j - g_i E_i - g_k E_k$$

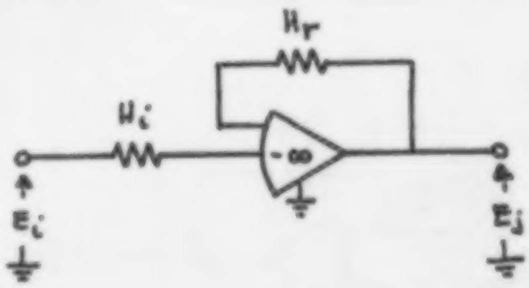
The $\underline{y}$ -matrix is then

$$\underline{y} = \begin{vmatrix} g_i & 0 & 0 \\ 0 & g_k & 0 \\ -g_i & -g_k & -g_f \end{vmatrix}$$

After the j-th row of the equation $\underline{I, I'}\rangle = \underline{G}\ \underline{E}\rangle$ has been set to zero, the operation $\underline{G} = \underline{G} \oplus \underline{y}$ is performed. By the same reasoning as above any number of inputs may be added to a scalor, differentiator, or accumulator.

Scalor (Mnemonic SC).

Diagram



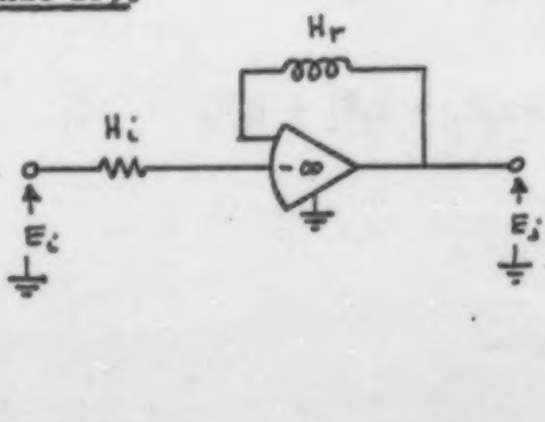
(conductance)

Definitive equation

$$E_j = -\frac{H_i}{H_r} E_j$$

Differentiator (Mnemonic DF).

Diagram

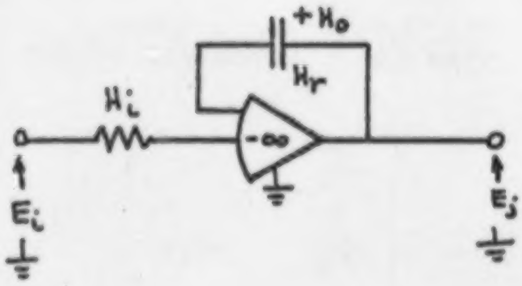


Definitive equation

$$E_j = -\frac{H_i}{H_r} sE_i$$

Accumulator or Integrator (Mnemonic AC).

Diagram



(conductance, capacitance, volts)

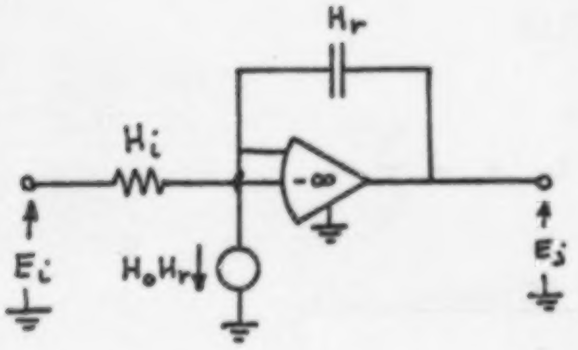
Definitive equation

$$E_j = -\frac{H_i}{H_r}\left(\frac{1}{s}\right) E_i + \frac{H_o}{s}$$

Because the accumulator may have an initial voltage (H_o), this element must be handled in a slightly different manner. The definitive equation is rewritten

$$-(H_r)(H_o) = -H_r sE_j - H_i E_i$$

Thus showing that the initial voltage may be replaced with an impulse source of value $-(H_o)(H_r)$. The diagram of the circuit is, for this configuration



(H_i) (H_r) $(H_o H_r)$
(conductance, capacitance, charge)

By this procedure, not only is the y -matrix of the accumulator; namely

$$\begin{array}{c}i\\j\end{array}\begin{bmatrix} H_i & 0 \\ -H_i & -H_r s \end{bmatrix}$$

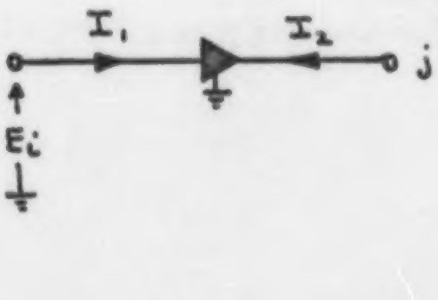
added to the G -matrix, but also the j-th entry of the initial-condition source column of the matrix I,I'> is changed to the value $-(H_r)(H_o)$; that is, the j-th row of I,I'> and G eventually look like

$$|0 - (H_f)(H_o)| \text{ and } \begin{array}{|cccccccc|} \overset{1}{0} & \overset{2}{0} & \cdots & \overset{i}{-H_i} & \cdots & \overset{j}{-H_f s} & \cdots & \overset{n}{0} \end{array}$$

The accumulator may have more than one input, but there may be only one initial condition.

Unistor (Mnemonic UN).

Diagram



Definitive equations

$$I_i = H_i E_i$$

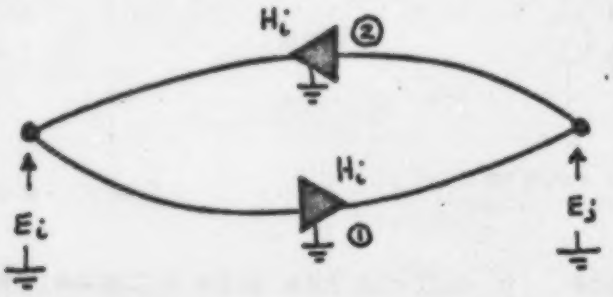
$$I_j = -H_i E_i$$

The $\underline{y}$-matrix for the unistor is, from the equations

$$\underline{y} = \begin{vmatrix} H_i & 0 \\ -H_i & 0 \end{vmatrix}$$

Unlike the operational amplifier elements, the unistor has its $\underline{y}$-matrix added directly to the $\underline{G}$-matrix; that is, the j-th row of the matrix equation is not set to zero.

It is worth noting that two unistors, when placed back-to-back, form a two-terminal conductance. The configuration for this is



The two $\underline{y}$-matrices are

$$① \begin{array}{c} \begin{array}{cc} i & j \end{array} \\ \begin{vmatrix} H_i & 0 \\ -H_i & 0 \end{vmatrix} \end{array} \quad \text{and} \quad ② \begin{array}{c} \begin{array}{cc} i & j \end{array} \\ \begin{vmatrix} 0 & -H_i \\ 0 & H_i \end{vmatrix} \end{array}$$

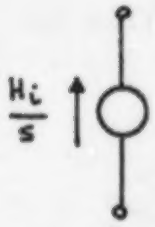
The sum $\underline{y}_1 \oplus \underline{y}_2$ is therefore

$$\begin{array}{cc} i & j \\ \end{array}$$
$$\begin{bmatrix} H_i & -H_i \\ -H_i & H_i \end{bmatrix}$$

which is identical to the matrix of the two-terminal conductance.

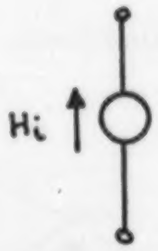
Sources.

There are two types of current sources which the designer may incorporate into his circuits: the step source (mnemonic ST) and the impulse source (mnemonic IM). Each source is characterized by one parameter H_i representing the current flowing from node i to node j through the source



(STEP SOURCE)

and



(IMPULSE SOURCE)

For either element, the $\underline{y}$ -matrix has zero entries everywhere, but their $\underline{I,I'\rangle}_y$ -matrices are

$$\begin{bmatrix} -H_i \frac{1}{s} + 0 \\ \\ H_i \frac{1}{s} + 0 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} -H_i + 0 \\ \\ H_i + 0 \end{bmatrix}$$

(step source) (impulse source)

The effect of either type is accounted for by the operation

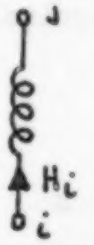
$$\underline{I,I'}\rangle = \underline{I,I'}\rangle \oplus \underline{I,I'}\rangle_y$$

Initial Conditions.

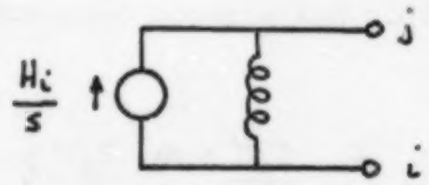
In order that the designer may specify non-zero initial conditions for the two-terminal inductance and two-terminal capacitance elements, the initial current and the initial voltage 'elements' have been provided. The data card containing the initial condition specifications must follow directly the card describing the element which is to have the initial condition.

Initial Current (Mnemonic IC).

The initial current element specifies the initial current H_i which is to flow from node i to node j through the inductance



This configuration is replaced with its Norton equivalent



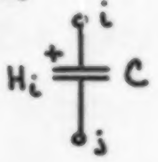
which behaves identically at the terminals. The effect of the inductance has already been accounted for, so that the $I,I'\rangle_y$ -matrix

$$\underline{I,I'}\rangle = \begin{bmatrix} 0 & -H_i/s \\ 0 & H_i/s \end{bmatrix}$$

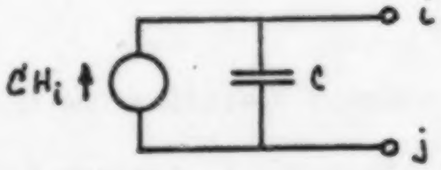
may be used to account for the initial current by the operation

$$\underline{I,I'}\rangle = \underline{I,I'}\rangle \oplus \underline{I,I'}\rangle_y$$

Initial Voltage (Mnemonic IV). The initial-voltage element is used to specify the initial voltage H_i on the two-terminal capacitor specified on the immediately preceding data card.



The configuration is replaced with its Norton equivalent



which behaves identically at the terminals. The $\underline{I,I'}\rangle_y$ -matrix is then

$$\underline{I,I'}\rangle_y = \begin{vmatrix} 0 & CH_i \\ 0 & -CH_i \end{vmatrix}$$

Since the effect of the capacitor has already been accounted for, the operation

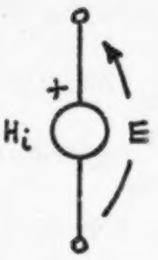
$$\underline{I,I'}\rangle = \underline{I,I'}\rangle \oplus \underline{I,I'}\rangle_y$$

accounts for the initial condition requirement, and hence for the entire configuration.

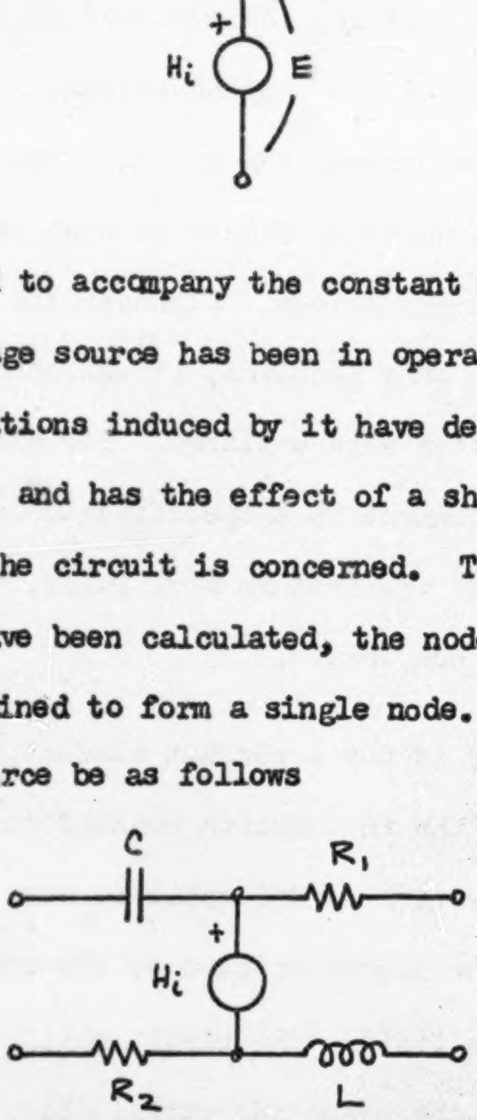
Voltage Source (Mnemonic VS). The voltage source element is characterized by the equation

$$E = H_i$$

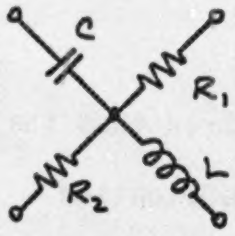
and by the diagram



This element was provided to accompany the constant node-voltage test. It is assumed that the voltage source has been in operation so long that the voltage and current variations induced by it have decayed to zero. The source is an ideal source and has the effect of a short-circuit, as far as the dynamic behavior of the circuit is concerned. Therefore, once the constant node-voltages have been calculated, the nodes between which the source is fastened are joined to form a single node. For example, let the circuitry involving a source be as follows



then, after the node-voltage test has been completed, the nodes are joined

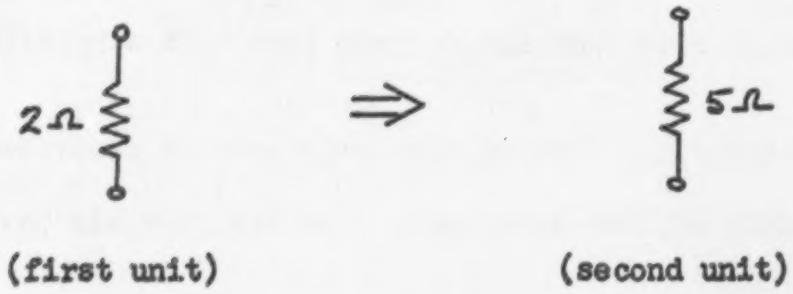


and the admittance equations are derived from this simplified configuration.

Underlined **Replication.** Before the last of the components is described, an additional feature of JOBSHOP will be mentioned. The designer may have his circuit replicated and tested several times, using only one deck of component cards. Originally this feature was incorporated to permit the designer to carry out tolerance investigations; that is, the designer would be able to specify a non-zero tolerance for any of his components; and then after the circuit has been replicated several times, the designer could compare the test results from the individual units to determine what percentage of the units were acceptable for his applications. Although the replication feature proved to be valuable for many problems, it was soon realized that there were more possibilities than were utilized. For example, one could not alter a parameter of an element by a specified amount without submitting the problem twice. To exploit the feature more fully, the augmentor was added to the list of available components.

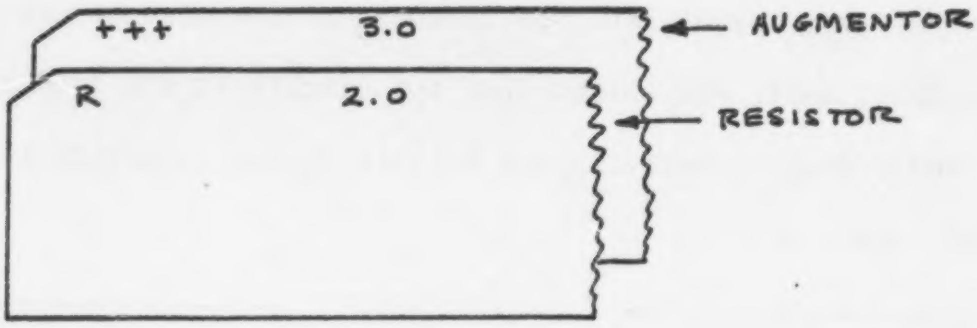
Augmentor. The augmentor is not a circuit element, but rather a code to the program, indicating that the information punched on the preceding card is to be altered. The alteration is accomplished after each replication, by adding the contents of the augmentor card to the contents of the preceding card, data field for data field. The result obtained from the alteration replaces the contents of the preceding card. Thus, one may use the augmentor to alter the parameters of components, and also to alter the parameters of other augmentors.

For example, it is desired that the 2-ohm resistor be changed to a 5-ohm resistor on the first replication



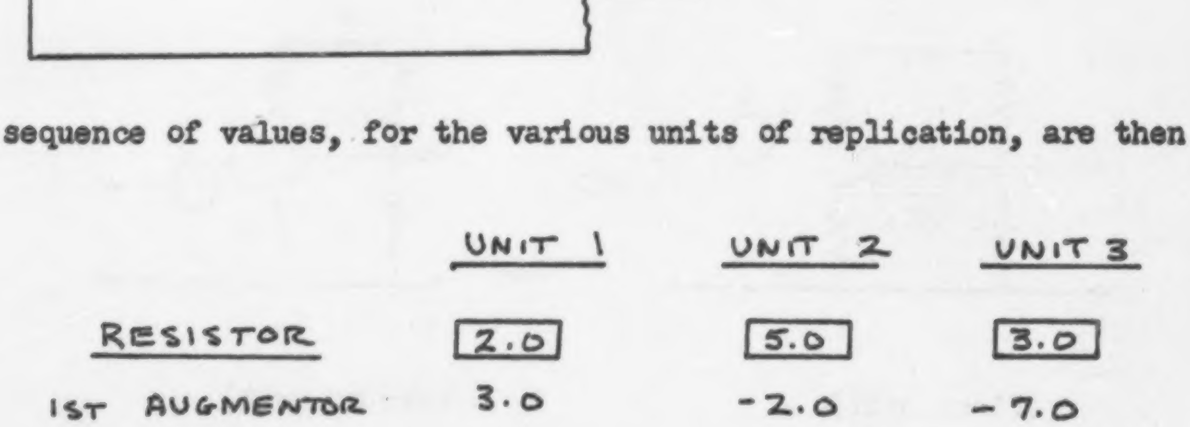
(first unit) (second unit)

The designer punches a card representing the 2-ohm resistor (i.e., a card with $H_1 = 2.0$) and follows this card with an augmentor having $H_1 = 3.0$. The cards would look somewhat like the following


+++
3.0
AUGMENTOR
R
2.0
RESISTOR

For the first unit, the resistor has the value of 2-ohms, on the second unit or first replication, the value of the resistor is $2.0 + 3.0 = 5.0$.

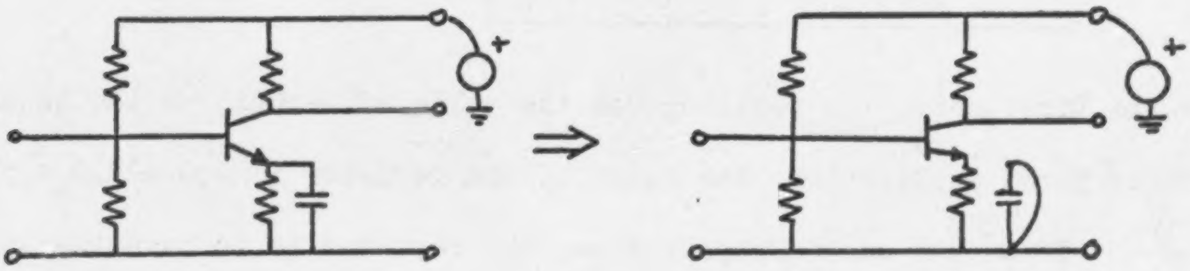
If on the second replication, the resistor is to have the value of 3.0 ohms, a second augmentor is used, having $H_1 = -5.0$.


+++
-5.0
2ND AUGMENTOR
+++
3.0
1ST AUGMENTOR
R
2.0
RESISTOR

The sequence of values, for the various units of replication, are then

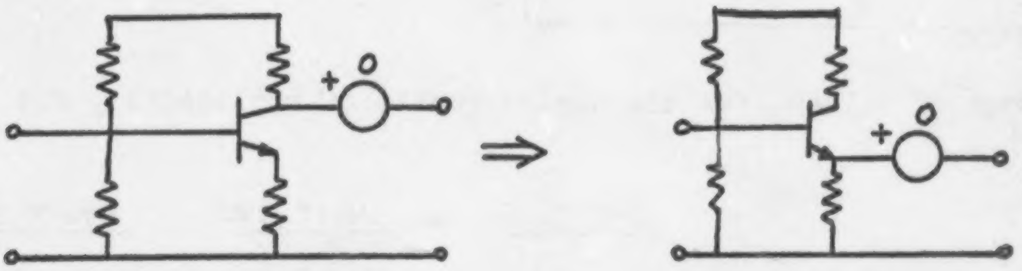
	UNIT 1	UNIT 2	UNIT 3
RESISTOR	$\boxed{2.0}$	$\boxed{5.0}$	$\boxed{3.0}$
1ST AUGMENTOR	3.0	-2.0	-7.0
2ND AUGMENTOR	-5.0	-5.0	-5.0

The augmentor may be used to alter any of the other parameters of the element except its mnemonic. For example, the nodes to which the element is fastened may be changed on successive units of a lot. By altering the nodes, the designer may investigate the behavior of the circuit with elements present in the first unit, and absent from the circuit in the second unit. For instance, the effect of removing the emitter bypass capacitor is readily studied, viz.



(first unit)　　　　　　(second unit)

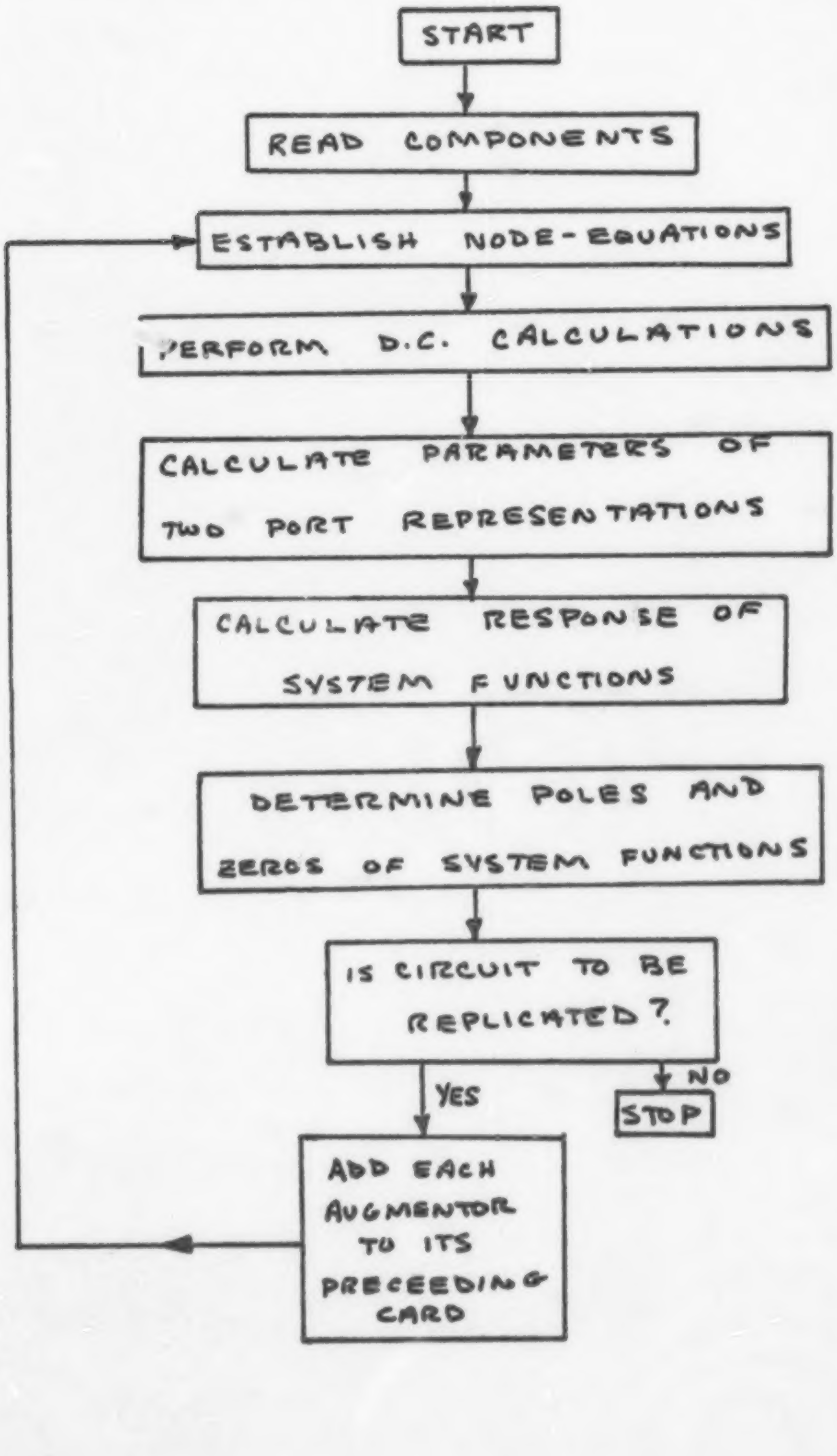
The augmentor may also be used to alter the input and output nodes in successive units of replication to investigate all possible transfer functions of a given circuit. Here, the voltage source, with zero voltage, is used as a moveable "cliplead" since this element has the effect of a short circuit



(first unit)　　　　　　(second unit)

These examples, by no means, exhaust the possible uses of the augmentor.

Summary. There are many facets of JOBSHOP which have not been discussed here, but all of the basic principles making JOBSHOP a realizeable program have been presented. To summarize these basics and to review the logic incorporated in JOBSHOP, the following flow-chart ends the discussion.


START
READ COMPONENTS
ESTABLISH NODE-EQUATIONS
PERFORM D.C. CALCULATIONS
CALCULATE PARAMETERS OF TWO PORT REPRESENTATIONS
CALCULATE RESPONSE OF SYSTEM FUNCTIONS
DETERMINE POLES AND ZEROS OF SYSTEM FUNCTIONS
IS CIRCUIT TO BE REPLICATED?
YES
NO
STOP
ADD EACH AUGMENTOR TO ITS PRECEEDING CARD

SECTION II

Study of Educational Uses of the JOBSHOP Program

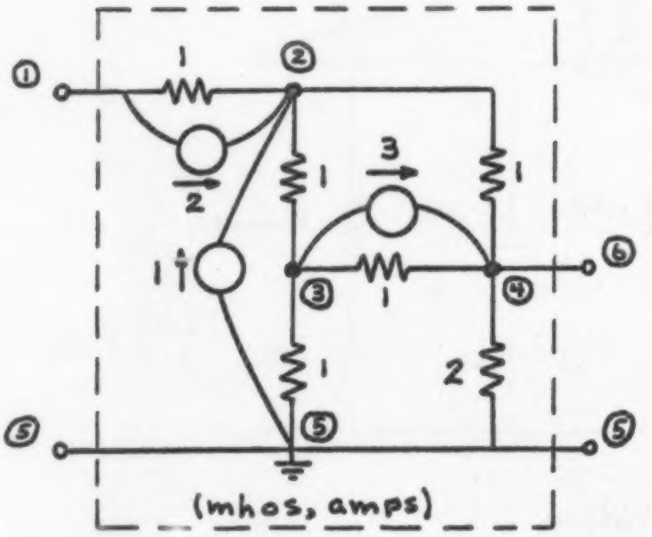
II.A. USE OF PROGRAM
IN INTRODUCTORY SYSTEMS AND
DESIGN, SPRING 1964

INTRODUCTION

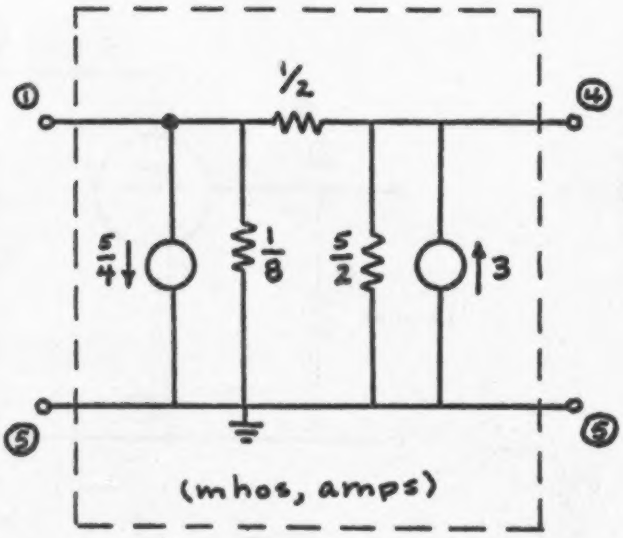
Early efforts (1962, 1963) to teach design principles by use of a circuit simulation program have already been mentioned in the introduction to this report. Generally, the conclusion was that the teaching effort was a profitable one, but of limited usefulness because truly interesting problems require dynamic elements. Accordingly, a more elaborate program was prepared, and its description is given in detail in Section IB and IC. An elaborate program requires elaborate support for efficient use. Specially prepared coding forms and descriptions for using the program have also been prepared (see Section IA and IB).

As of March 30, 1964, students in Introductory Systems and Design, a large undergraduate course, began using the elaborate JOBSHOP program. The first assignment concerned resistance networks with sources. It was aimed merely at acquainting the students with the mechanics of submitting requests, modifying requests, and interpreting diagnostic messages. Also by simultaneously solving circuits using pencil-and-paper vs. JOBSHOP, they were made aware of the advantages of computer solutions. The following problem was assigned:

Set up the node-pair equations for the circuit shown below at the left. By eliminating the "internal" nodes (2) and (3), show that this circuit is equivalent at its input and output terminals to the reduced circuit shown at the right below. The values of all sources are constants subsequent to t = 0.



Original Circuit



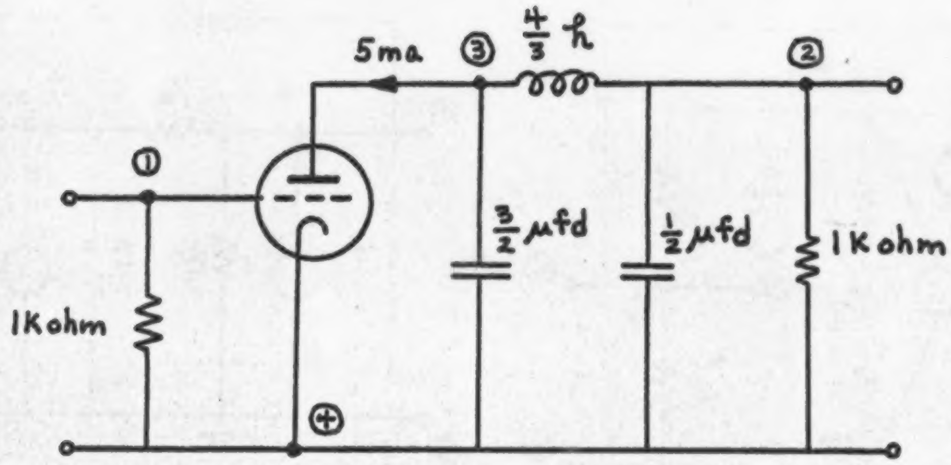
Reduced Circuit

1) Ask JOBSHOP to construct 3 replicas of this circuit. (Lot Size = 3). Request printout of node equations, punch equations, cost, two-port Y parameters, and two-port Z parameters, with input node = 1, output node = 4, ground node = 5, and serial number of first unit manufactured = 10. Compare your answers with Problem 2. Can you find a circuit involving three resistors and two voltage sources corresponding to the Z-parameters?

2) Repeat problem 3 but with 10-percent tolerances assigned to all conductances and a power rating of 2 watts.

* *

The second assignment dealt with a band-pass filter amplifier and was completed successfully by almost every student in the course. (A typical solution for this problem, as JOBSHOP output, follows at the end of this section.)



g = 5 millimhos

g_p = 0

1) Set up node admittance equations

2) Eliminate internal node to get A_{21}, Z_{11}, Z_{22}

3) Plot 50 pts., AMP, GAIN, REIM

freq. range: 0-2.5KCPS

4) Print the values of these functions at 5 selected frequencies in this interval.

5) Evaluate by hand calculation A_{21}, Z_{22}, Z_{11} at, at least, 2 different non-trivial frequencies in this range.

A typical JOBSHOP solution for this problem (omitting graphs) is included at the end of this section. The output differs slightly from its present form.

Another suggested problem (optional) concerned modification of a vacuum-tube filter to pass frequencies within only a specified range. This problem illustrated the ease with which successive parts of a design may be attached sequentially. The designer thus concentrates upon one facet of a problem and completes it before going on to a second facet.

These three problems, the text material prepared, and the supervision of JOBSHOP activities were significant accomplishments in the framework of the course, but did not permit sufficient data to be gathered pertinent to the main question being investigated: the capability of JOBSHOP as a teacher of electronic design. The sophomore students needed extensive training in the mechanics of submitting a design to the program and in circuit theory before meaningful design problems could be undertaken. Thus at the conclusion of the Introductory Systems course (June 1, 1964), we felt that these students were just about at a stage of development where extensive use could be made of the JOBSHOP program, and this led directly to the special summer sessions described in II.B. below.

SAMPLE PROBLEM — SPRING, 1964 — THE BUTTERWORTH AMPLIFIER

N.B. The computer output for this problem differs from the output for the examples in Section I.B. because further revisions, particular in printing details, were made in the JOBSHOP program after experience in the spring.

```
          HOMEWOOC ELECTRCNIC JCBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.        5/12/64

                              DATA INPUT
1111  577 1277 LYNCH,HUGH           BUTTERWORTH AMPLIFIER
ND IN GT GD LT  $ EC CD YS CD ZS CD FR TR                                SR MOD
 4  1  2  4  1 -0 -0 -0  1 -0  1 -0  1 -0                               5110-0

TYPE NC   I  J     HI     EXP RTNG TOL  K    HF          HR          HO       L
 G    1   1  4   1.CC000 -0  -C. -0. -0  -0.         -0.         -0.       -0
 G    2   2  4   1.CC000 -0  -0. -0. -0  -0.         -0.         -0.       -0
 L    1   3  2   1.33333 -0  -0. -0. -0  -0.         -0.         -0.       -0
 C    1   3  4   1.5CCC0 -0  -0. -0. -0  -0.         -0.         -0.       -0
 C    2   2  4   0.50000 -0  -0. -0. -0  -0.         -0.         -0.       -0
 G   50   1  3   0.      -0  -0. -0.  4   5.00000   0.          0.        -0
     -0  -0 -0   1.0C000 -0  -0. -0. -0  -0.         -0.         -0.       -0


                       TWO-PORT ADMITTANCE PARAMETERS

CHARACTERISTIC DENCMINATOR POLYNOMIAL IS
  0  0  3   0.7500CCE+0C S 0    0.              S 1    0.150000E+01 S 2  2

NUMERATOR POLYNOMIALS ARE
  I  J NH
  1  1  3   0.75000CE+0C S 0    0.              S 1    0.150000E+01 S 2  2

  2  1  3   0.3750CCE+01 S 0    0.              S 1    0.           S 2  2

  2  2  4   0.75000CE+0C S 0    0.150G00E+01 S 1    0.150000E+01 S 2  2
  2  2  4   0.750CCCE+0C S 3               +                  +         2


                       TWO-PORT IMPEDANCE PARAMETERS

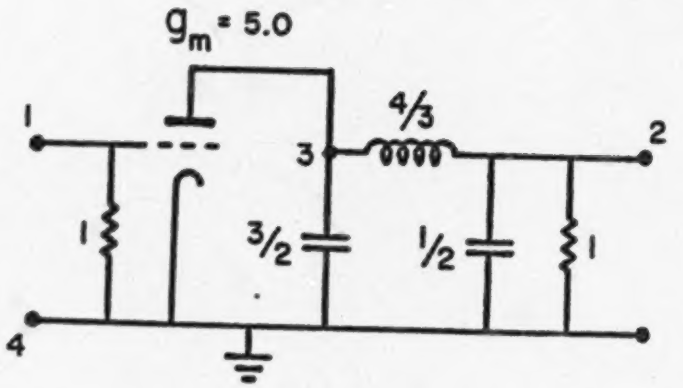
CHARACTERISTIC DENCMINATOR POLYNOMIAL IS
  0  0  4   0.7500CCE+0C S 0    0.150000E+01 S 1    0.150000E+01 S 2  3
  0  0  4   0.7500CCE+00 S 3               +                  +         3

NUMERATOR CF OPEN-CKT IMPED Z( 1 1)  IS
  1  1  4   0.7500CCE+0C S 0    0.150C00E+01 S 1    0.150000E+01 S 2  3
  1  1  4   0.750CCCE+0C S 3               +                  +         3

NUMERATOR OF OPEN-CKT IMPED Z( 2 1)  IS
  2  1  3  -0.3750CCE+01 S 0   -0.              S 1   -0.           S 2  3

NUMERATOR OF OPEN-CKT IMPED Z( 1 2)  IS

NUMERATOR OF OPEN-CKT IMPED Z( 2 2)  IS
  2  2  3   0.7500CCE+0C S 0    0.              S 1    0.150000E+01 S 2  3
```



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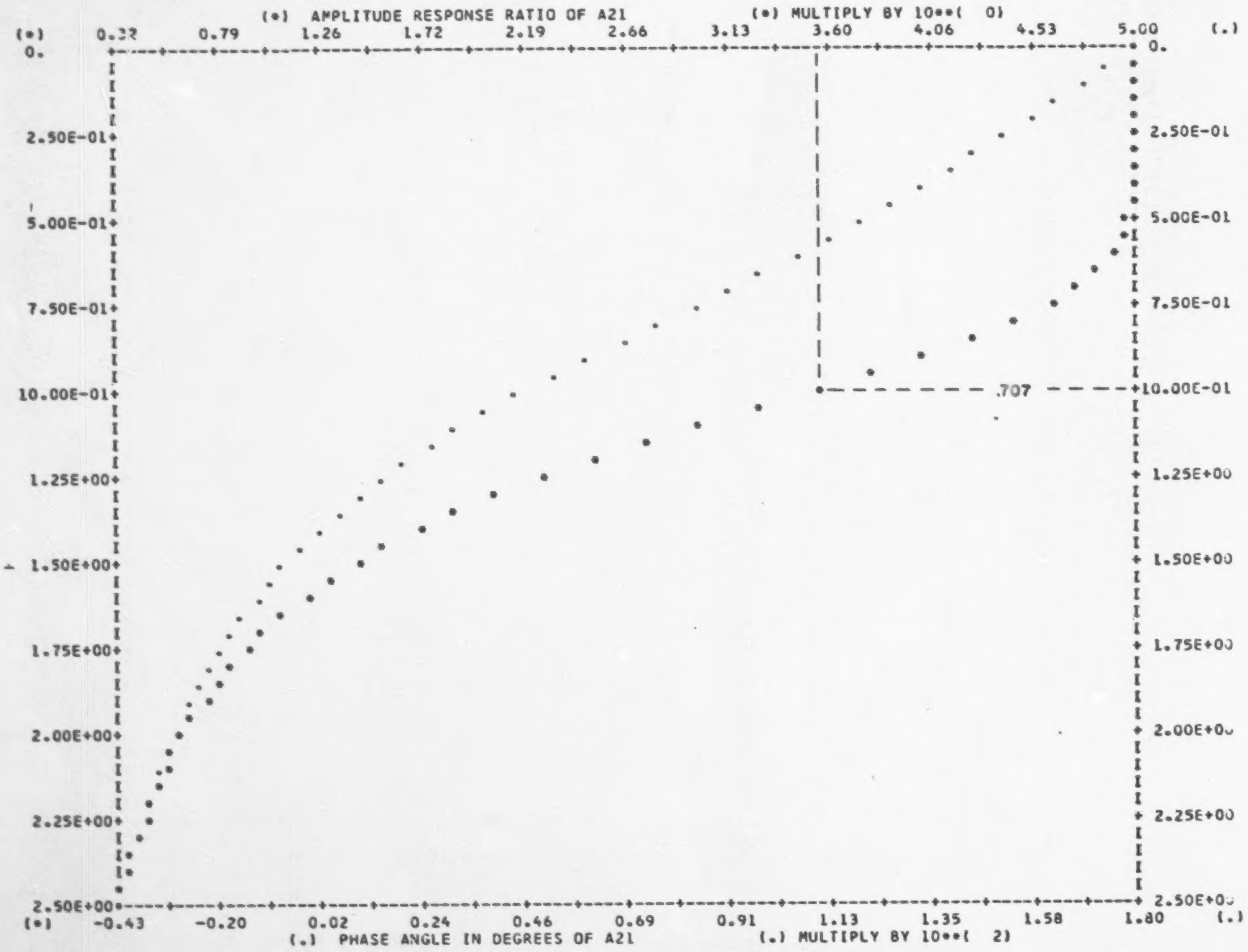
        HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.        5/12/64

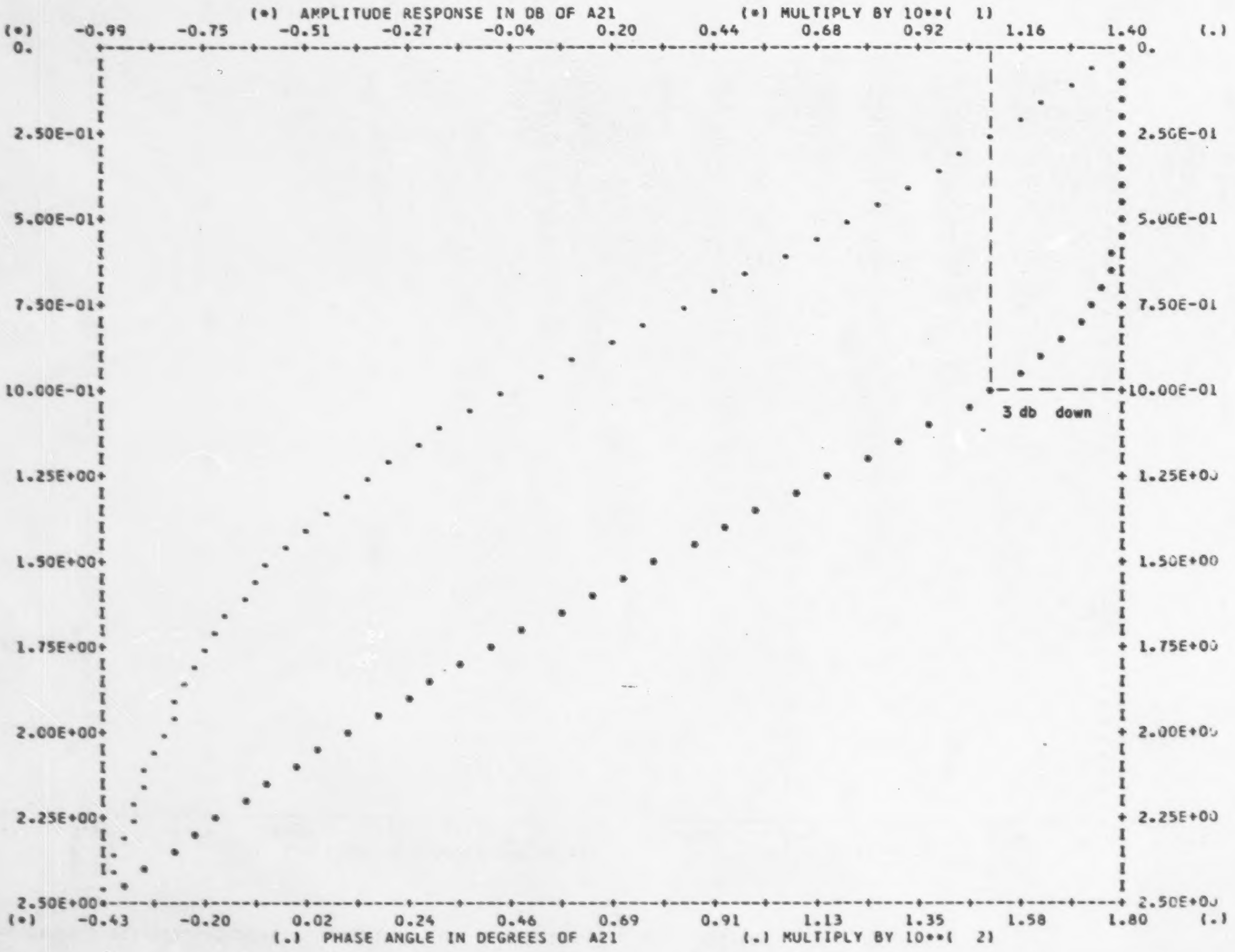

                FREQUENCY RESPONSE CHARACTERISTICS

L     FQMIN    MEXP CPS NINCR  LOG  FQMAX     AMPL GAIN ANGL REIM PRNT
1  0.            -0   -0   50   -0  2.500000    1    1    1    1   -0
1  A21   Z11   Z22   -0   -0   -0
```

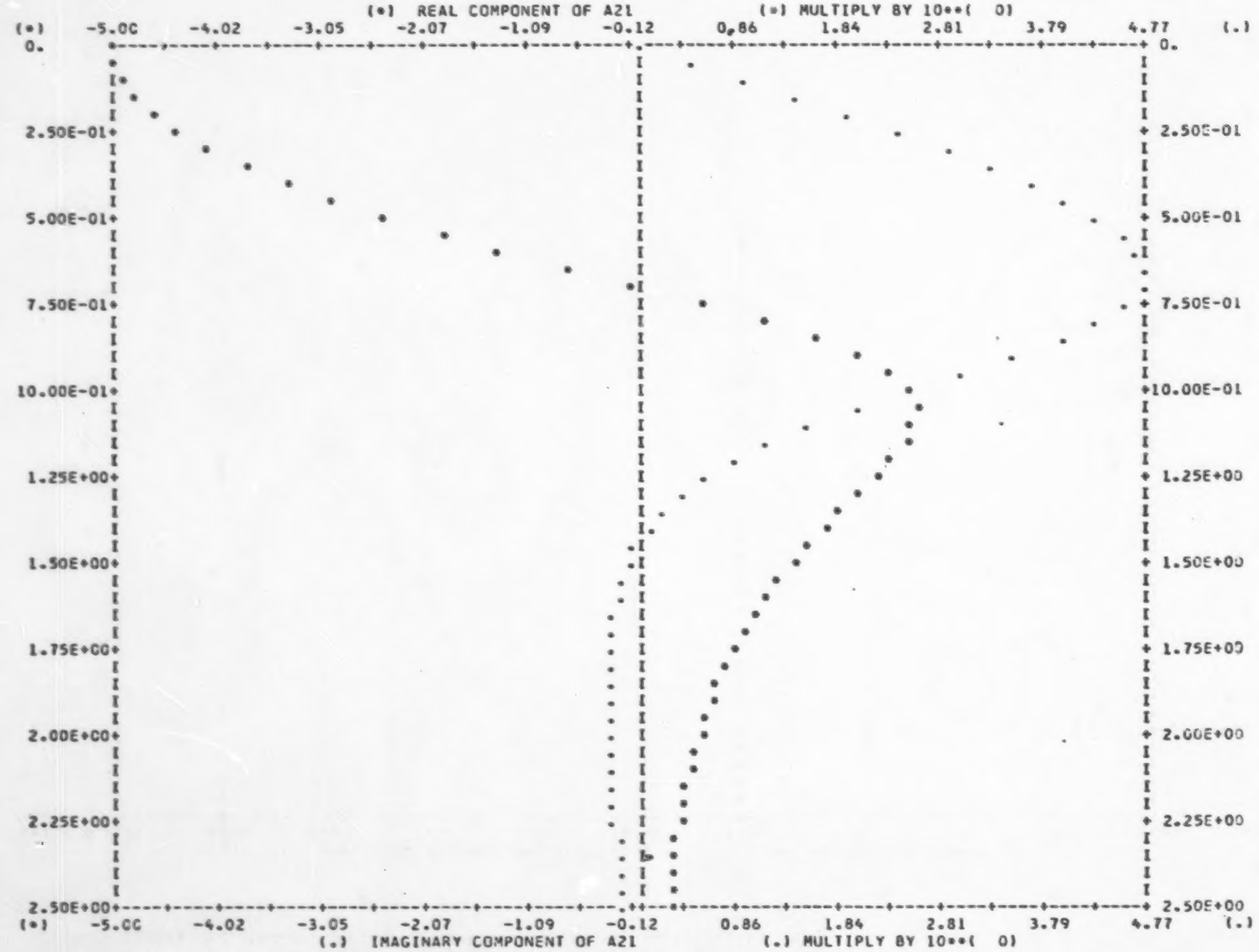
MCPEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.   5/12/64



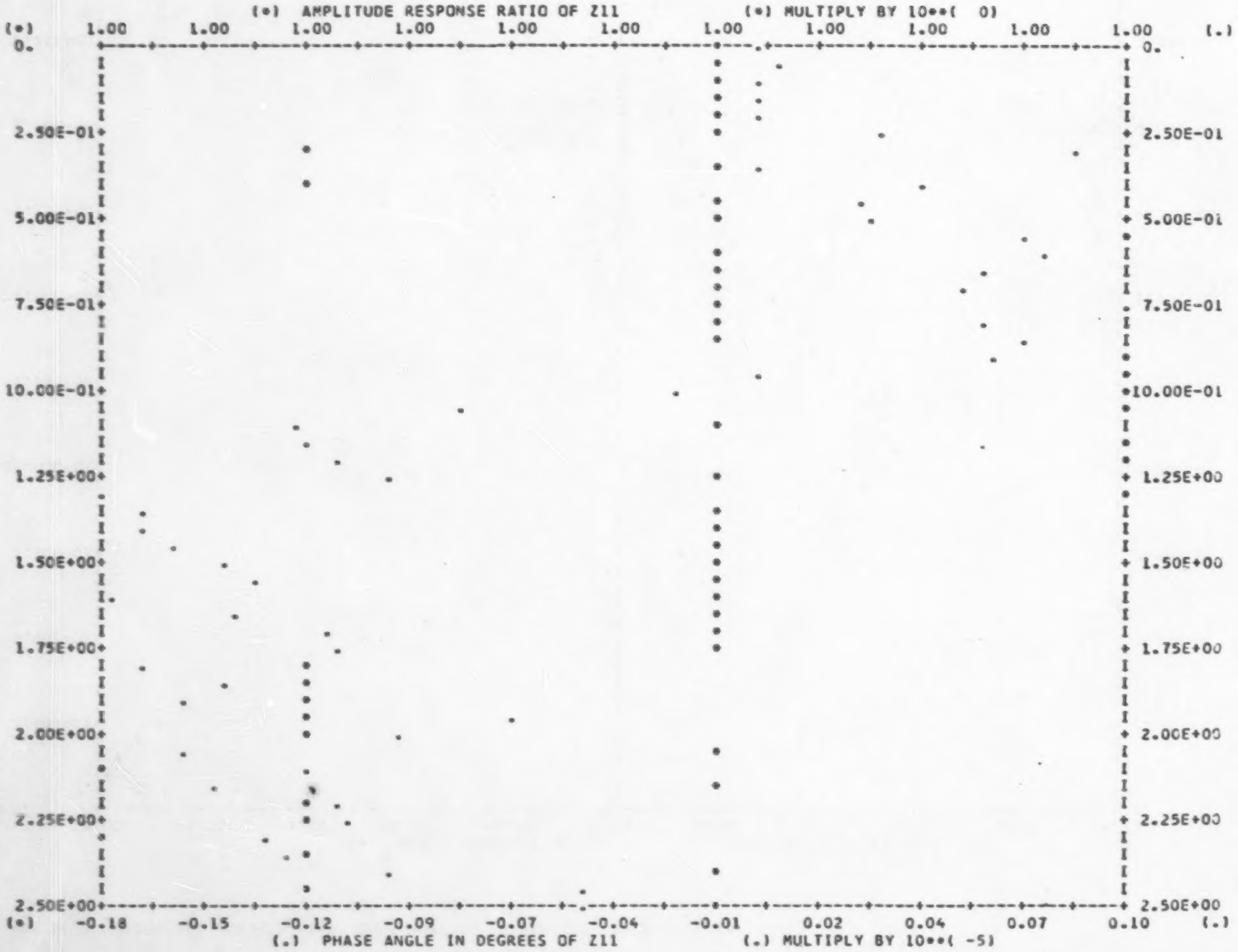
HCMEWOOD ELECTRCNIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.   5/12/64



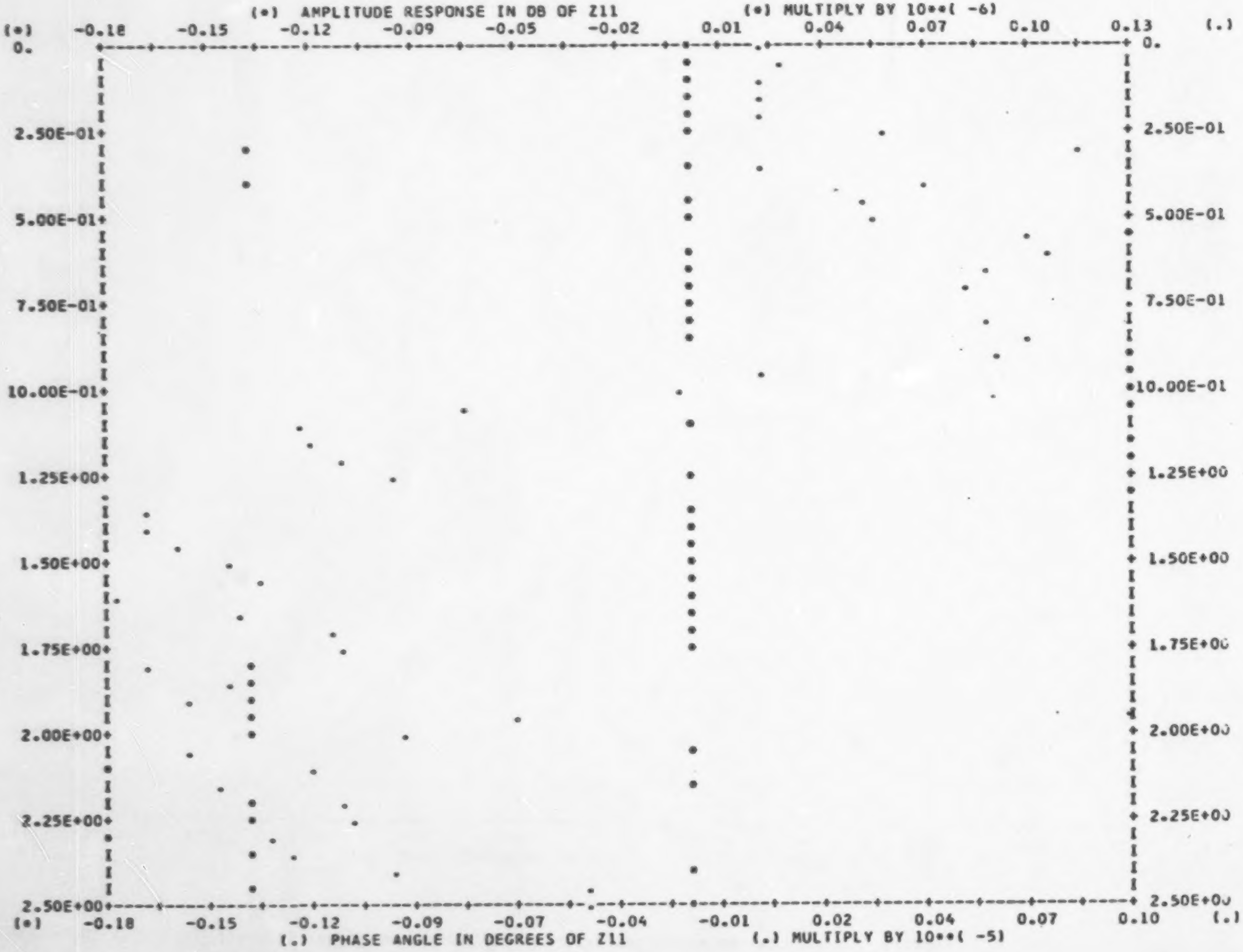
HCPEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.   5/12/64



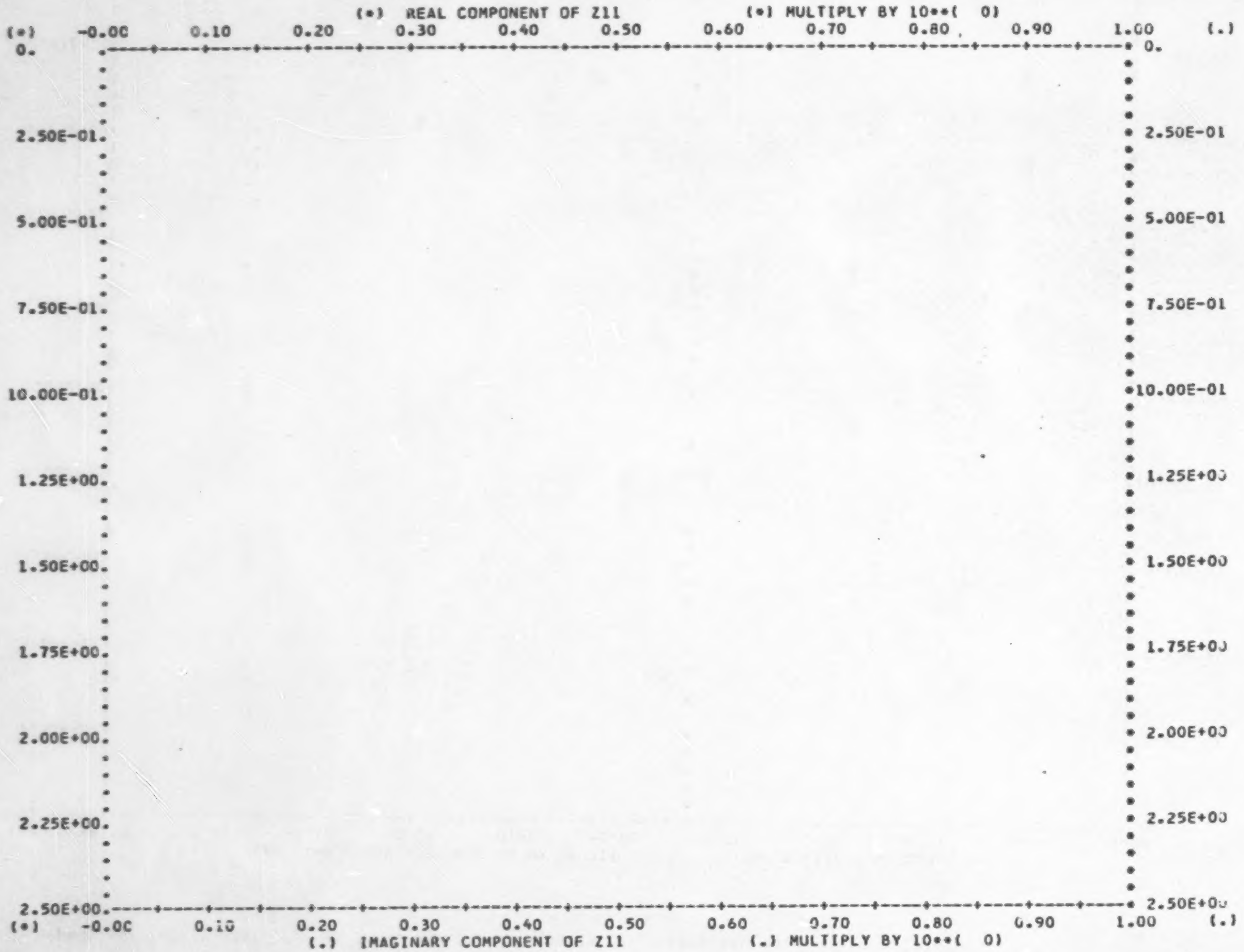
HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD. 5/12/64



HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD. 5/12/64



HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD. 5/12/64



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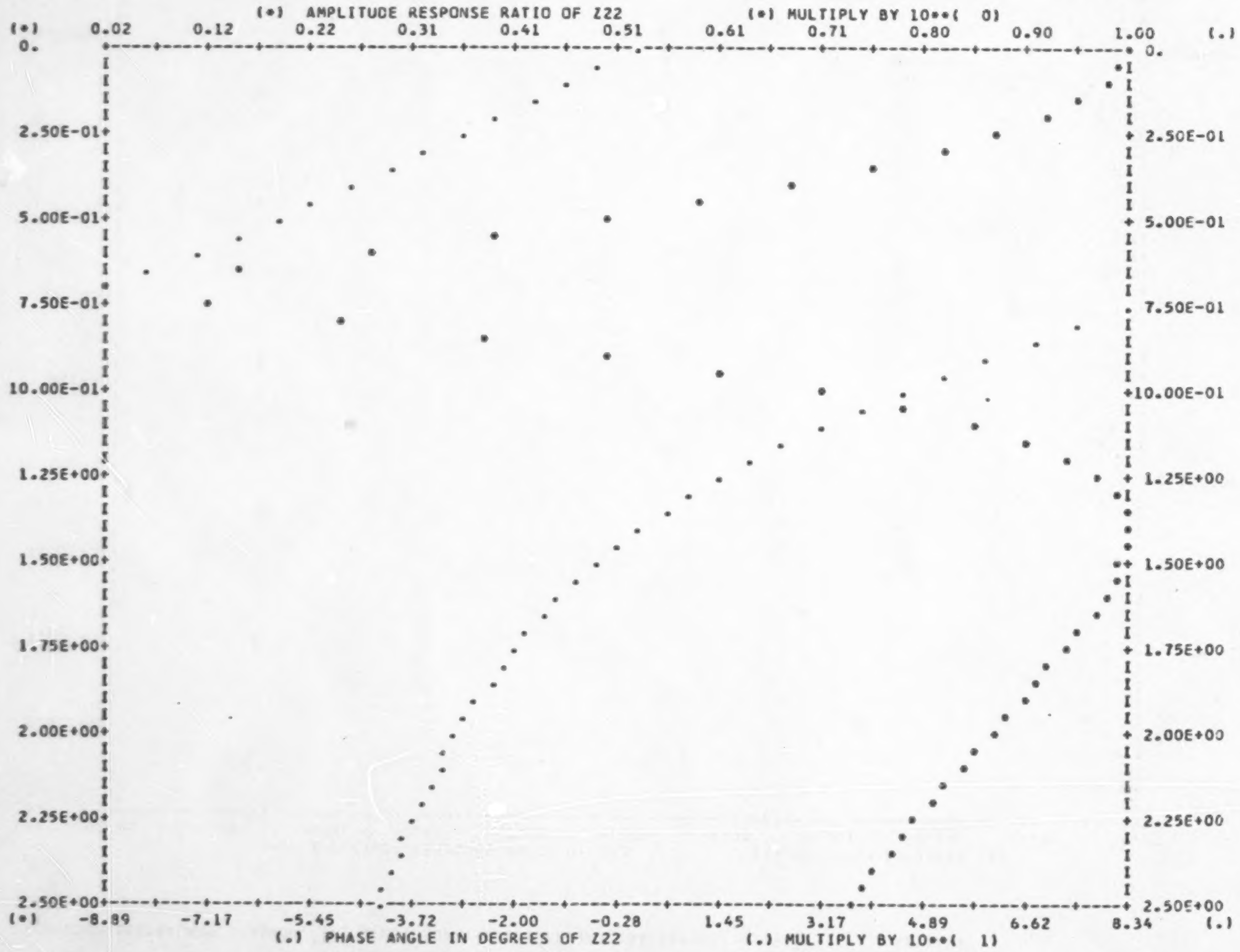

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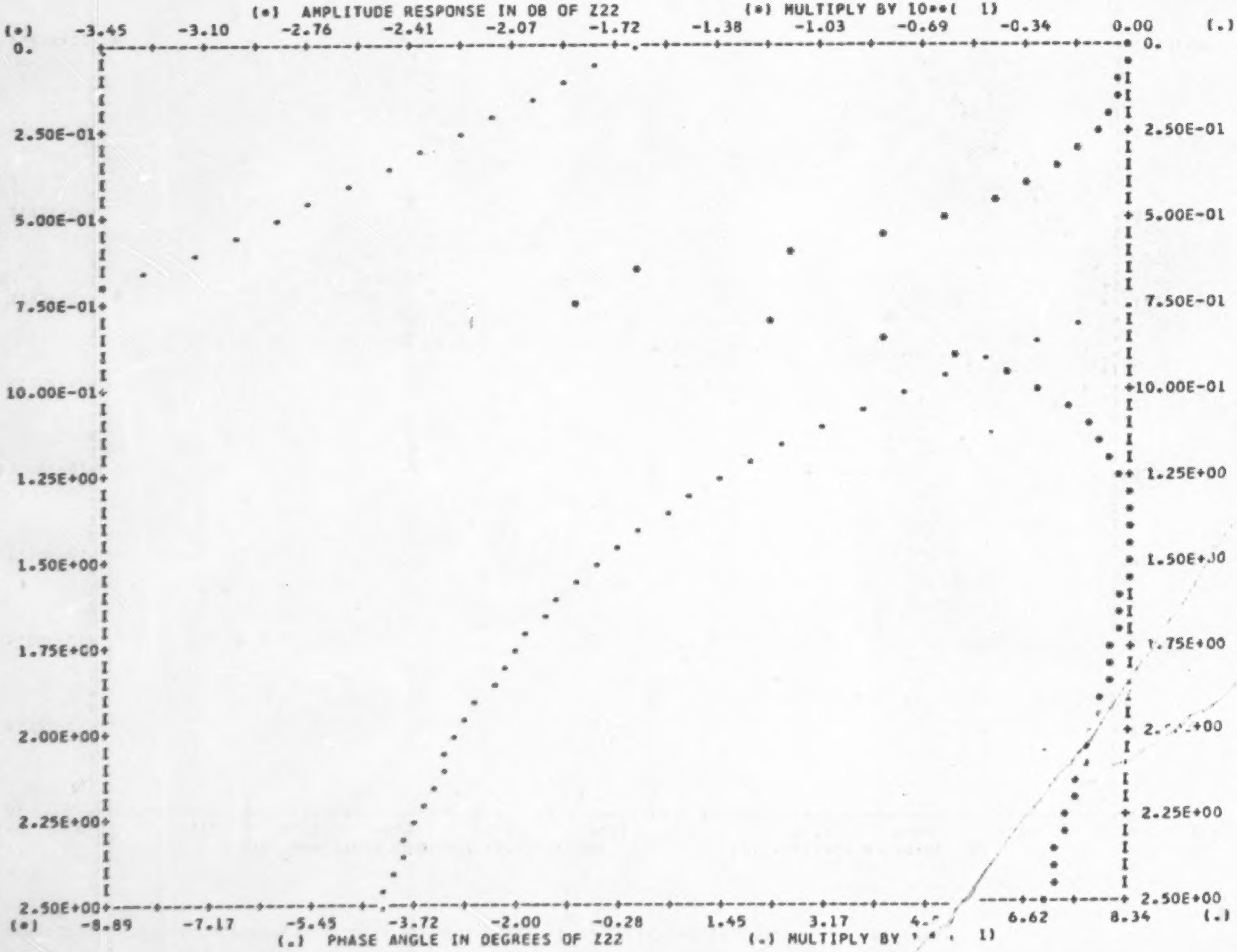

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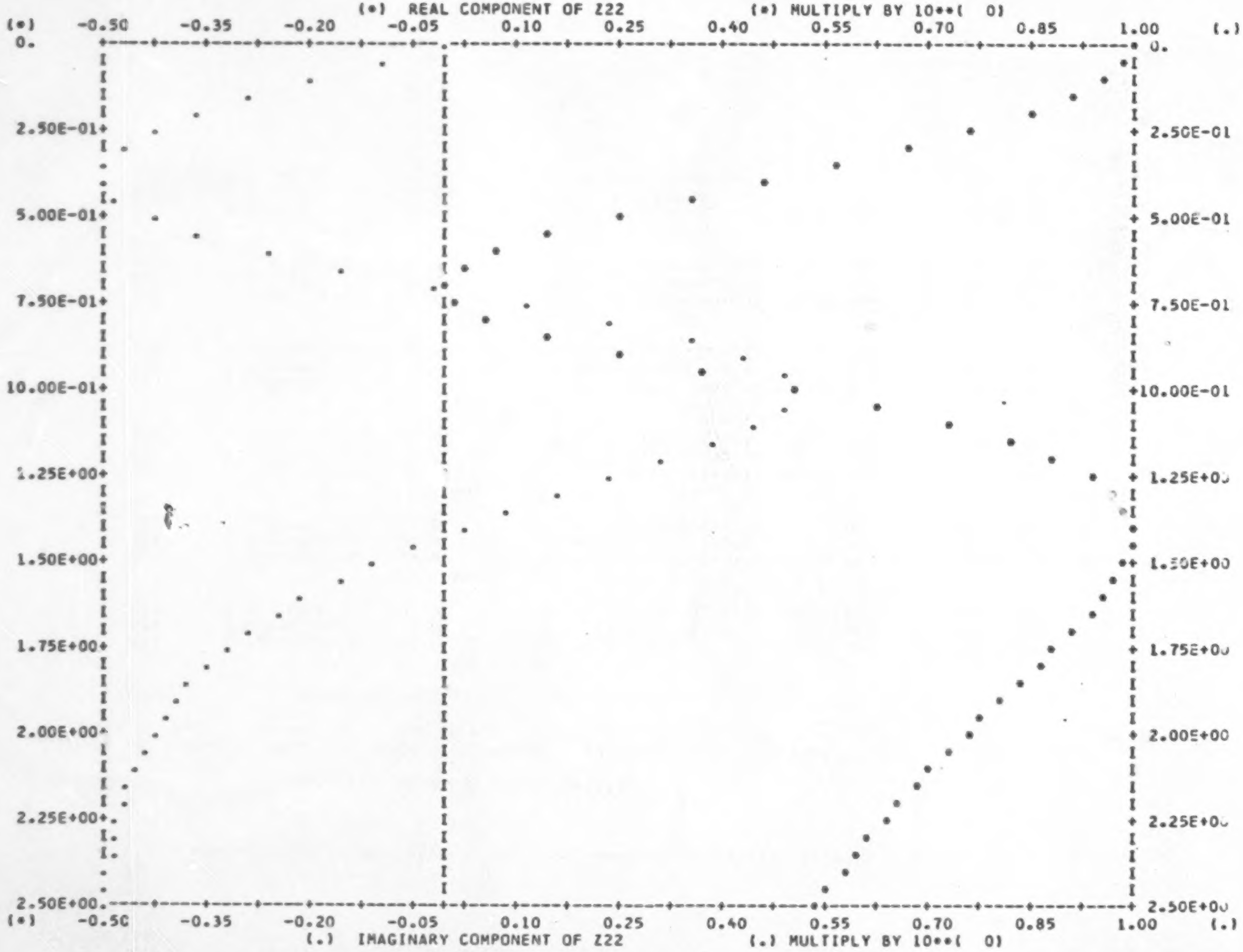

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HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.         5/12/64


                FREQUENCY RESPONSE CHARACTERISTICS

 L     FQMIN   MEXP CPS NINCR  LOG  FQMAX     AMPL GAIN ANGL REIM PRNT
 1  0.          -0   -0    5   -0 -0.          -0   -0   -0   -0    1

PHASOR          FREQUENCY IN RAD/SEC,     IN CYCLES/SEC

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.

                  0.            RPS     0.             CPS
 A21      (-0.50000E+01) + J(-0.          )  =  ( 0.50000E+01)/ 180.00 DEG        13.98 DB.
 Z11      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
 Z22      ( 0.10000E+01) + J( 0.          )  =  ( 0.10000E+01)/   0.   DEG        -0.   DB.
```

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HOMEWOOD ELECTRONIC JOBSHOP, THE JOHNS HOPKINS UNIVERSITY, BALTIMORE 18, MD.        5/12/64

          I N V O I C E   F O R   E L E C T R O N I C   U N I T S   M A N U F A C T U R E D

SOLD TO  LYNCH,HUGH              STUDENT IDENT. NUMBER   577             INVOICE DATE  5/12/64

 ITEM   YOUR ORDER  SERIAL              DESCRIPTION                          COST OF MANUFACTURE
NUMBER    NUMBER    NUMBER                                          PARTS    ASSEMBLY   TESTS      TOTAL

  1        1277      5110   BUTTERWORTH AMPLIFIER                   72.10     100.65     17.10     189.85

                                                                    TOTAL AMOUNT OF INVOICE $      189.85
```

II.B. THE SUMMER JOBSHOP SESSIONS, JUNE, JULY, 1964

When experience indicated that use of the JOBSHOP simulation with sophomores enrolled in Introductory Systems and Design would not provide as much information as we required to evaluate the program, it was decided to embark on a special summer teaching program of 9 weeks' duration. The purpose of the summer program was to work intensively with students, and in a sense to see how much electronic design could be taught to them in a short period of time with the help of the JOBSHOP program.

There are several ways to evaluate the success of this effort:

(1) An evaluation of the group's progress in nine weeks and comparison of this progress with experience in teaching conventional courses. This is necessarily subjective, but the kinds of problems worked on can be roughly equated to material in courses.

(2) A comparison of the students' performance on a specific problem with performance on the same problem by experienced designers. There are two comparisons here: (a) A D-C coupled amplifier problem (see Section II.B.1) and (b) a problem (see Section II.B.2).

(3) A systematic study of the opinions of the students themselves (see Section II.B.3).

(4) Other individual and in-course uses of the JOBSHOP simulation for other kinds of students.

The Sessions, June 1 - July 31, 1964. A group of students was assembled who had maintained grades no less than C in Introductory Systems and who had taken the course in 1963-64 or 1962-63.* They were required to spend a minimum of four hours daily, five days a week, for the nine-week JOBSHOP research session. Plans were flexible, but generally about half the time was spent in classroom work, and the other half spent in laboratory sessions. The laboratory consisted entirely of attempts to solve assigned problems in design using the JOBSHOP program. Time was required to translate problems into designs that could be simulated in JOBSHOP, the submission of the data to the computation center for punching and checking (some students preferred to do their own keypunching), and then analysis of results and modification of designs in terms of previous results. A typical problem would be submitted 3 or 4 times (see Section B. for average figures on this).

For the most part, Professor W. H. Huggins led the formal class discussions. Considerable reliance was placed on Electronic Circuits by E. J. Angelo, Jr. (McGraw-Hill Book Co., New York: 1964), and Poles-Zero Patterns (E. J. Angelo, Jr. & A. Papoulis. McGraw-Hill, 1964). All students were provided copies of these references and problems in these books were used. A systematic statement of the problems assigned and results secured is given below in the Before-After Comparison of the Summer Students.

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*Seven had grades of C, five had B, and 10 had earned A's.

II. B.1 BEFORE-AFTER COMPARISON OF GROUP: THE STUDENTS' PROGRESS OVER THE NINE-WEEK PERIOD OF THE SUMMER RESEARCH PROGRAM

Introduction and Purpose of Section II.B.1.

The first task was to develop a coding sheet on which the pertinent data concerning the assigned problems could be put in a condensed form. A coding sheet was used for each student and for each problem. A sample copy of this form is given as Figure B.1.1.

Examination of the material revealed that there were fifteen problems which the majority of the students had worked. These were the problems on which data were taken. A list of these problems is given at the end of this section. A problem number was assigned to each problem. For brevity, these numbers will be used to refer to the problems in all data in this report. Of these fifteen problems assigned in lecture, seven were taken from Electronic Circuits, E. J. Angelo, Jr., McGraw-Hill Book Company, Inc., 1964. This was used as a text for referral.

Table B.1.1 presents a list of available data, consisting of all JOBSHOP output and analytical calculations turned in by the students. The purpose of this list is to show what information is available for analysis. In particular, these data permit the selection of two problems, one from the beginning and one from the end of the session, to be used to determine how the student's approach to problems and use of JOBSHOP changed throughout the session. These are presented in Section II.B.2.

Next is an error analysis, in Table B.1.2. This reveals how long the students took to adapt to the program. Coding errors are not segregated from key-unching errors, because not many JOBSHOP coding forms were turned in by the students. It was hard to tell if errors occurred during coding or key-punching. The data showing how successful the students were in getting jobs to run throughout the session may be found in Table B.1.2. Table B.1.3 gives a break-down of the sources of error in using the program. These data have guided revision of the JOBSHOP coding form and the instructions explaining the use of the program (Sections I.A and I.B).

The next part of the report is an examination of the various kinds of information requested from JOBSHOP by the students throughout the sessions, such as what phasors, functions, or voltages were called for. The data also show what frequency scale (logarithmic or linear) and what frequency units (CPS or RPS) were used by the students. These data show trends in the information the students tended to rely upon as the course progressed and as the ability of the students' in solving the problems changed. These data may be found in Tables B.1.4, B.1.5, B.1.6.

Following the above, interpretations of the data are given.

Figure B.1.1. Problem analysis outline

PROBLEM____

A. Analytical Calculations YES__________ NO__________

1. Preliminary, for the purpose of:

a. Analysis YES__________ NO__________

b. Design YES__________ NO__________

2. After JOBSHOP results have been received for the purpose of

a. Re-Analysis YES__________ NO__________

b. Re-Design YES__________ NO__________

3. JOBSHOP data used for calculations

Nodal voltages and currents________________________________.

Component voltages and currents____________________________

Cost of parts______________________________________

Response curves: Amp.________, Gain________, REIM________________

Angl________, Print____________.

Node-Pair Equations________, Y and Z equivalent circuits.

____

4. Uses of JOBSHOP:

a. Tolerance investigation: YES__________ NO__________

Single Component__________________Circuit__________________

b. Augmentation of component: YES__________ NO__________

To study the effect of_______________________________________

____

c. D.C. voltages and currents called for: YES________ NO__________

Nodes____________________ Components______________________

d. Cost of parts: YES________ NO________

e. Frequency Responses called for AMP.________ Gain________

REIM.________ ANG.________ PRINT________

f. Verification of design: YES________ NO________

g. Analysis: YES________ NO________

h. Frequency Scale: CPS________RPS________ LOG________LINEAR________

i. Functions called for:____

____

j. Poles and Zeros: YES________ NO________

k. Modify: YES________ NO________

l. Other uses and remarks:

Table B.1.1

Available Data

Problem No.	(1) Attempted Problem	(2) Preliminary Calculations	(3) Calculations Using JOBSHOP Results	(4) JOBSHOP Results
1.)	17	8	13	17
2.)	20	15	15	20
3.)	19	14	11	19
4.)	17	16	11	17
5.)	20	14	14	20
6.)	10	7	6	10
7.)	12	11	9	12
8.)	20	10	15	20
9.)	22	10	20	22
10.)	22	19	21	22
11.)	22	18	19	20
12.)	13	11	10	13
13.)	15	13	11	15
14.)	16	14	10	12
15.)	22	21	3	16

All numbers refer to the number of students who (1) attempted the problem, (2) did preliminary calculations, (3) did calculations after JOBSHOP runs using information from JOBSHOP output, and (4) received further (second-round) JOBSHOP results (satisfactory or unsatisfactory).

Table B.1.2

Error Analysis Data

	Jobs			Lots		
Problem Number	Total	Successful	% Successful	Total	Successful	% Successful
1.)*	21	18	85.7%	41	34	83.0%
2.)	52	31	59.6%	153	84	55.2%
3.)	52	30	57.7%	219	84	38.7%
4.)	55	30	54.7%	73	43	59.0%
5.)	48	30	62. %	177	107	60.4%
6.)	15	10	66.7%	25	17	68.0%
7.)	20	14	70.0%	52	35	67.4%
8.)	35	26	74.3%	35	26	74.3%
9.)	128	122	95.3%	932	876	94.0%
10.)*	56	51	91.0%	230	216	94.0%
11.)	44	39	88.5%	104	85	81.5%
12.)	32	26	81.0%	52	40	77.0%
13.)	37	35	94.6%	50	48	96.0%
14.)	17	17	100.0%	17	17	100.0%
15.)	36	30	83.5%	36	27	73.0%
Static	253	221	87.3%	1380	1233	89.5%
Dynamic	395	288	73.0%	816	506	62.0%
Total	648	509	78.5%	2196	1739	79.3%

*Denotes a static, or non-frequency dependent problem.

Table B.1.3

Error Analysis - Errors Made Using JOBSHOP

Per-cent values refer to the per-cent of total errors that are accounted for by a particular error.

I. Errors involving nodes - Total - 35%

  A. Node left floating above ground causing admittance matrix to be singular - 6.1%

  B. Component connected to wrong node - 15.4%

  C. Node number punched in wrong column causing node number to exceed NNODES - 13.8%

II. Errors involving components - Total - 23%

  A. Used H parameters instead of L parameters for transformer - 2.3%

  B. Put parameters (HI, HF, HR, HO) in wrong column - 3.8%

  C. Operational Amplifier connected wrong (backwards or floating above ground) - 5.4%

  D. Left Vacuum Tube out of circuit - 1.5%

  E. Left out common node of vacuum tube - 6.1%

  F. Current source put in wrong (Backwards or floating above ground)- 4.6%

  G. Forgot SNORM card - 0.1%

III. Augmentation errors - Total - 5%

IV. Phasor and Function Errors - Total - 37%

  A. Didn't have set of phasor and function cards for each lot - 10.8%

  B. Set NINRC - 0. - 3.1%

  C. Didn't punch FR (phasors) - 9.2%

Table B.1.3 (Continued)

D. Didn't have blank cards for each lot between sets of phasor and function cards and 1 blank card/lot plus 1 extra at end of program - 5.4%

E. Bad AMN selection card (usually punched in wrong column or function called for which isn't in the library) - 2.3%

F. Order of phasor and function cards reversed - 2.3%

G. Bad use of transients (forgot to punch TR or had transient card wrong) - 1.55%

H. Bad phasor cards (punched in wrong column) - 3.0%

Data Requested from JOBSHOP by Users:

The following tables show what information was requested by the users of JOBSHOP throughout the course.

All numbers refer to the number of students.

Table B.1.4

Currents, Voltages, Cost of Parts, Equations and Parameters

Problem	Received Computer Results	Cost Parts	Node Voltages, Currents	Component Voltages, Currents	Node Equations	Y, Z Parameters
1.)	17	17	17	17	13	13
2.)	20	19	19	19	16	16
3.)	19	19	19	19	13	13
4.)	17	17	17	17	14	14
5.)	20	20	20	20	10	10
6.)	10	10	10	10	7	7
7.)	12	12	12	12	5	5
8.)	20	18	16	16	14	13
9.)	22	22	22	22	7	6
10.)	22	22	22	22	3	3
11.)	20	14	12	12	8	9
12.)	13	10	9	9	3	4
13.)	15	11	10	10	4	4
14.)	12	9	5	5	5	3
15.)	16	12	6	6	3	3
Totals	255	232	216	216	125	124

Table B.1.5

Phasors
(All numbers refer to the number of students)

		Phasors Asked for:				
Problem	Received Computed Results	Gain	Amp	Angl	Print	REIM
1.)	17	0	0	0	0	0
2.)	20	17	10	17	6	5
3.)	19	10	16	16	9	2
4.)	17	17	17	17	6	8
5.)	20	0	0	0	0	0
6.)	10	4	5	5	3	1
7.)	12	0	4	4	4	1
8.)	20	14	19	19	7	20
9.)	22	1	1	1	1	0
10.)	22	0	0	0	0	0
11.)	20	20	15	20	2	1
12.)	13	12	6	12	1	3
13.)	15	15	7	15	3	2
14.)	12	9	5	9	0	1
15.)	16	10	5	10	3	1
Totals	255	129	103	145	45	45

Table B.1.6

Frequency and Frequency Scale
(All numbers refer to the number of students)

Problem	Received Computer Results	Frequency Units CPS	RPS	Scale Log	Linear
1.)	17	0	0	0	0
2.)	20	16	3	14	5
3.)	19	16	0	4	12
4.)	17	15	2	17	0
5.)	20	0	0	0	0
6.)	10	4	1	0	5
7.)	12	3	0	0	3
8.)	20	2	18	20	0
9.)	22	1	0	1	0
10.)	22	0	0	0	0
11.)	20	9	12	17	4
12.)	13	10	2	8	4
13.)	15	12	2	10	4
14.)	12	5	3	7	1
15.)	16	11	0	5	6
Totals	255	104	43	103	44

Discussion and Conclusions:

The best problems for comparison in order to study the changes in the students' approach to problems and their changes in the use of JOBSHOP are problems two, three, or four vis-a-vis problem eleven (the Miller Effect). The problems deal with analysis as, opposed to design, and are frequency-dependent problems and hence, required the use of phasors on JOBSHOP. Also, there is a large amount of material - in comparison to other problems - available on these problems for analysis and study.

The design problems best suited for comparison are those where students and consultants are compared. The error analysis data show two significant trends. First, the ability of the students to get jobs to run successfully increased by a factor of almost two as the course progressed. The final design problem showed a drop-off in performance, probably because there was much tension on the student's part to get this problem completed before the end of the course. (Also the computer was down at several points during the final week of our summer session.) The increases in performance as the sessions progressed and the figure of nearly 80% successful jobs and lots are most encouraging signs. The data show that the students' success in getting static or non-frequency dependent problems to run successfully was much greater than their success in getting frequency dependent problems to run. This is because more errors were made in calling for phasors and functions on a frequency dependent problem. The re-design of the coding form should do much to eliminate this source of trouble.

The summary of errors made in using the program, especially errors involving nodes, can be attributed to carelessness on the part of the coder or key-punch operator. Errors involving the wrong connection of components, especially current sources, operational amplifiers, and tubes, will probably be alleviated to some extent by a revision of the instruction sheet. The instructions have since been re-worded to show the proper connection of certain components, and this is carefully explained in the instruction sheet. There were some errors which occurred because the common node of a vacuum tube or operational amplifier or other three-terminal devices were left out. This error is now less likely because the K-node column was moved next to the I-node and J-node columns. The fact that a set of phasor and function cards is needed for each lot is now made clear in the instructions. This was a very common source of error. Another fact made clearer now in the instructions is that a blank card between each set of phasor and function cards and one blank card per lot plus one extra card at the end of the program is needed. This was another common source of error. There was some error in having the order of the phasor and function cards wrong. The coding form has been changed so that the lines for phasors and functions are alternated. There was some error in the correct manner of augmentation, and the instructions are now clearer on this point. The remaining errors represent only a small per-cent of the total errors and their cause is chiefly carelessness.

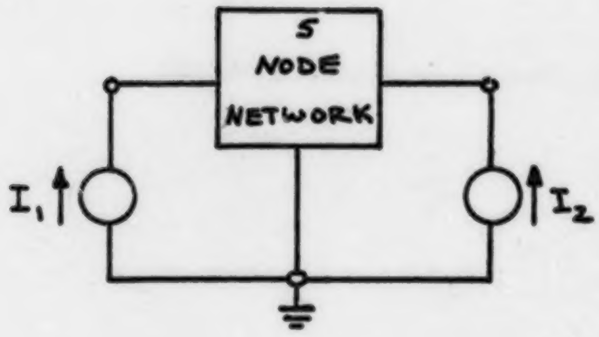
The nature of the problems reveals that the material covered is complex and difficult. The mere fact that so many problems (15) could be worked several times over suggests that a large part of the computational burden was assumed by the computer. Also the list of problems, beginning with a simple resistance network, progressing through a series of dynamic as well as static problems, and culminating in the kind of problem given last (a wide band amplifier to use with a microelectrode) more than any other single piece of evidence attests to the actual achievement of the students. It is extremely doubtful that either the amount of material included or the difficulty level of the problems would have been the same without the practice-possibilities afforded by JOBSHOP.

In judging the achievement of these students, it should be recognized that prior to this experience, most of them have had little or no experience with electronic circuits *per se*. Their previous course, Introductory Systems and Designs, deals primarily with ideal (computer-like), systems and only incidentally with electric circuits, although the basic concepts of linearity, equivalent systems, transfer functions, and frequency response are introduced. Furthermore, none of the sophomores had studied physical electronics. Despite this, the students found the design problems meaningful and made satisfactory progress toward their solution. The final design problem, of a special multistage amplifier having a response that would compensate for the deficiencies of a specified input circuit, involved concepts normally encountered in graduate courses on circuit design. Yet many of the students made substantial progress toward completing this problem.

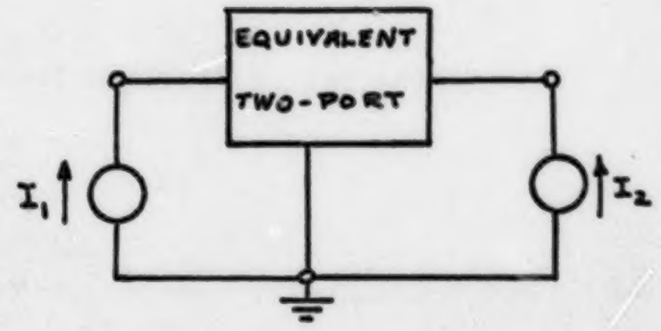
The Set of Problems Used in the Summer Research Program

Problem No. 1 - Resistance Network - June 1, 1964

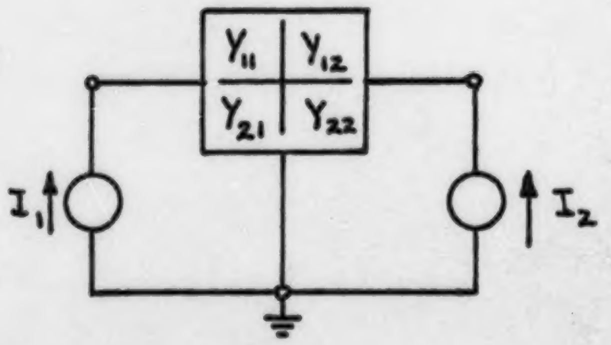
Construct a simple resistance network having five nodes (including datum or ground node.) and two step current sources (Inport, Outport). Reduce this circuit to equivalent two-port and find the Thevenin and Norton equivalent circuits. Have JOBSHOP build and analyze the circuit in order to check your analytical results.


5
NODE
NETWORK
I_1
I_2

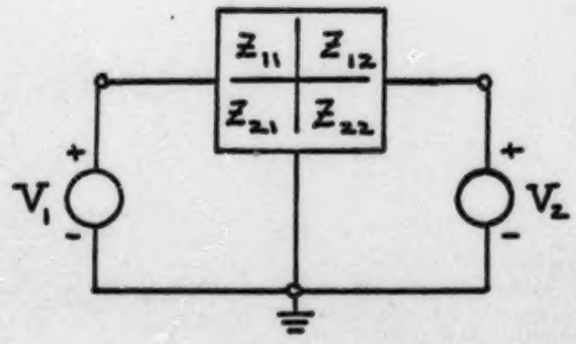
ORIGINAL CIRCUIT


⇒
EQUIVALENT
TWO-PORT
I_1
I_2

EQUIVALENT TWO-PORT


Y_{11}
Y_{12}
Y_{21}
Y_{22}
I_1
I_2

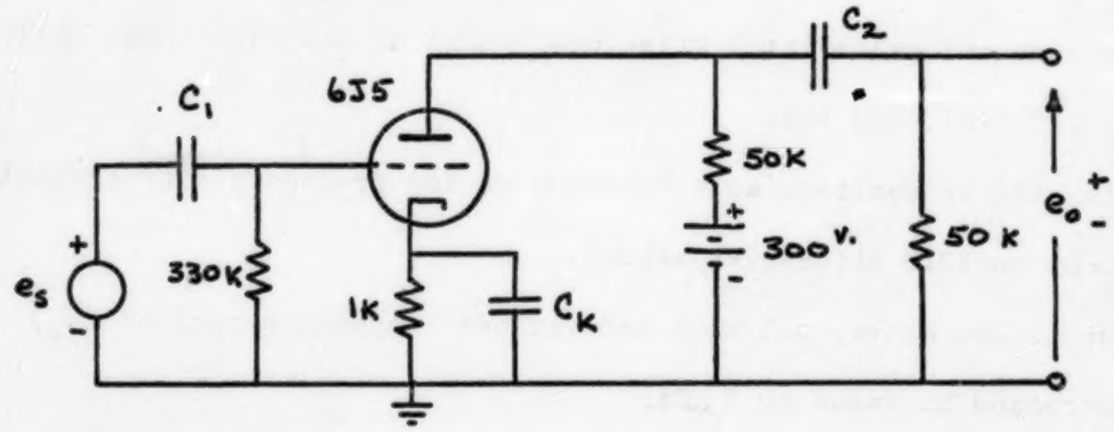
NORTON EQUIVALENT


⇒
Z_{11}
Z_{12}
Z_{21}
Z_{22}
+
V_1
-
+
V_2
-

THEVENIN EQUIVALENT

Problem No. 2 - Angelo 6-5, page 173, Fig. 6-17 - Effect of the bypass capacitor on gain.

Part A. - Analytical solution (from text)



Taken from Angelo, p. 173.

a. Construct the static load line and locate the quiescent operating point.

b. Construct the dynamic operating path, assuming $I_b = I_{b_o}$ so that this path passes through the quiescent point.

c. For linear Class A1 operation, the dynamic operating point should not go into the positive grid region and it should not go below the i_b = 1 ma line. Subject to these restrictions, what is the greatest amplitude that a sinusodial input signal can have?

d. What is the maximum amplitude of the output voltage that can be obtained from the amplifier under the conditions of part C?

Part B. - JOBSHOP Simulation (given by Dr. Huggins) with reference to figure 6-17, let $C_1 = 0.01\mu$fd, $C_2 = 0.1\mu$fd, $C_k = 20\mu$ fd ± 20%. Also assume that for the 6J5 tube, $g_m/g_p = \mu = 20$, $g_p = 1/r_p = 0.1$ mmho. (Note: the actual characteristics are given on page 635 of text.)

1.) Have JOBSHOP build the circuit in Fig. 6-17.

2.) Use an equivalent Norton circuit for the plate supply and find the d-c operating voltages and currents.

3.) Measure the values at 1 kilocycle/second of the functions Z11, Z22, A21, and A12.

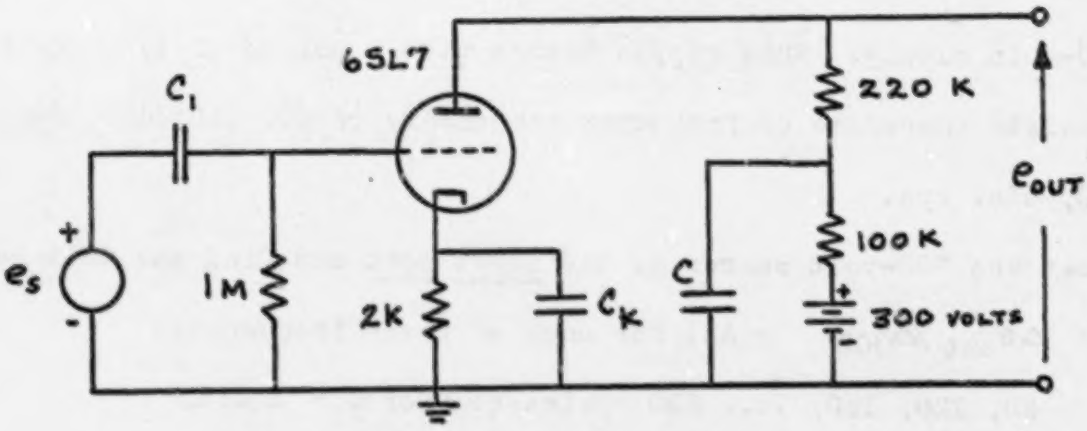
4.) Plot A21 in decibels as a function of log frequency over the interval 0.001 to 10.0 kilocycles/second.

5.) Repeat the above, but with the cathode - bypass capacitor (C_k) decreased in value to 2 μfd.

6.) Repeat but with the cathode bypass capacitor reduced to zero value (i.e. removed entirely).

Problem No. 3 - Angelo 6-6, pages 173-179, Fig. 6-18 - Elimination of ripple.

Part A. - Analytical solution (from text).



Taken from Angelo, Fig. 19-18.

In high-gain multistage amplifiers it is usually necessary to use decoupling networks, like that formed by the 100 - kilohm resistor and capacitor C in the circuit of Fig. 6-18, to reduce interaction among the stages. The effect of the decoupling network on the procedure of graphical analysis is to be examined.

a. Sketch the static load line on the e_b, i_b coordinates, and locate the quiescent operating point. The plate characteristic curves can be obtained from this sketch.

b. Add the dynamic operating path to the sketch of part a, making the assumption that $I_b = I_{b_0}$. A simple procedure is to pass a line having the proper slope through the quiescent point. Indicate the voltage at which this path intersects the e_b axis.

Part B - JOBSHOP Simulation (given by Dr. Huggins); with reference to Fig. 6-18, let $C_1 = 0.01 \mu fd$, $C_k = 20 \mu fd$. Also assume $\mu = 60$,

g = 0.02 mmhos.

1.) Have JOBSHOP build the circuit shown in Fig. 6-18 in which we wish to investigate the effectiveness of the decoupling capacitor C in isolating and filtering out the ripple voltage that is present on the 300-volt supply. This ripple occurs with a period of 1/60 second and consists therefore of frequency components of 60, 120, 180, 240, 300, 360, etc. cps.

2.) Treat the 300-volt source as the input port and find the voltage ratio

$\Delta e_{out} / \Delta_{300}$ = A21 for each of these frequencies

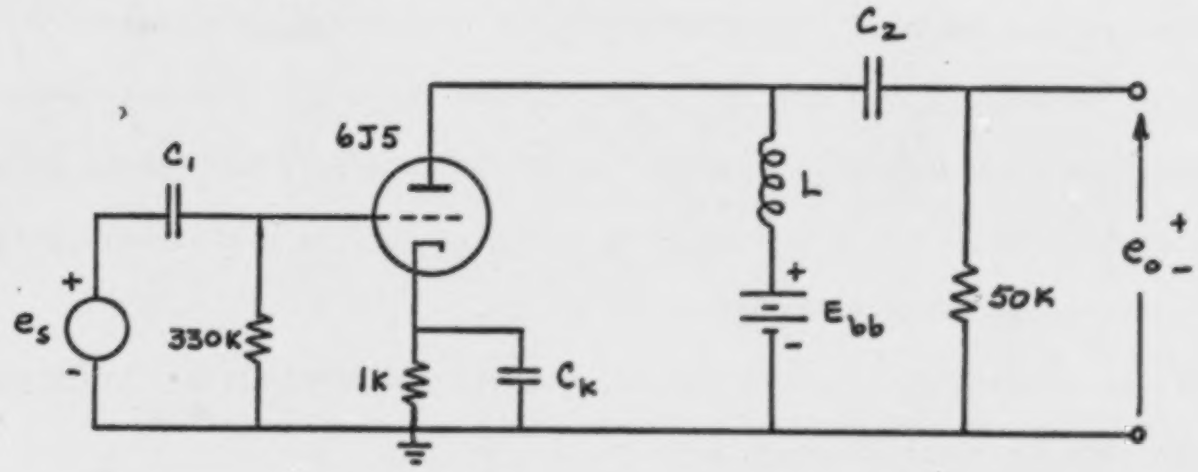
60, 120, 180, ... 600 cycles/sec for C = 4 μfd.

3.) Repeat the above measurements but with the 20 μfd cathode-by-pass capacitor removed completely. Does this capacitor affect the output ripple signal?

4.) If the power supply voltage had a sinusodial ripple of 1 volt peak amplitude of frequency of 120 cps, what value of C would be necessary to reduce the ripple in the output signal e_{out} to less than 1 millivolt?

Problem No. 4 - Angelo 6-7, page 174, Fig. 6-19 - Effect of inductance in the plate load.

Part A - Analytical Solution (from Text).



Taken from Angelo, p. 174.

The amplifier shown in Fig. 6-19 is identical with the one shown in Fig. 6-17 except that the plate load resistor is replaced with an inductor. With this arrangement the plate supply voltage required for a given quiescent point is smaller than in the circuit of Fig. 6-17, and slightly higher gain is obtained; on the other hand, the size, weight, and cost are greater, and, as a rule, the performance is poorer at very high and very low frequencies. Certain features of this amplifier are to be examined by graphical analysis.

a. The quiescent operating point for the amplifier in Fig. 6-17 is approximately at i_b = 4 ma and e_c = -4 volts. Assuming that the inductor has negligible resistance, what value of Ebb is required to give this quiescent point in the amplifier of Fig. 6-19? Compare this result with the plate-supply voltage used in the circuit of Fig. 6-17.

b. Sketch the static load line and the dynamic operating path on the Cb, in coordinates. Assume that the inductor acts as an open circuit and the capacitors act as short circuits to the time varying components of current and voltage. The characteristic curves can by omitted from this sketch, but the voltage at which each operating path intersects the C_b axis should be indicated. A simple procedure for constructing the dynamic operating path when $I_b = I_{b_o}$ is to pass a line having the proper slope through the quiescent point.

c. If the input signal is sinusoidal, what is the greatest amplitude it can have in class A_1 operation?

Part B - JOBSHOP Simulation (Given by Dr. Huggins).

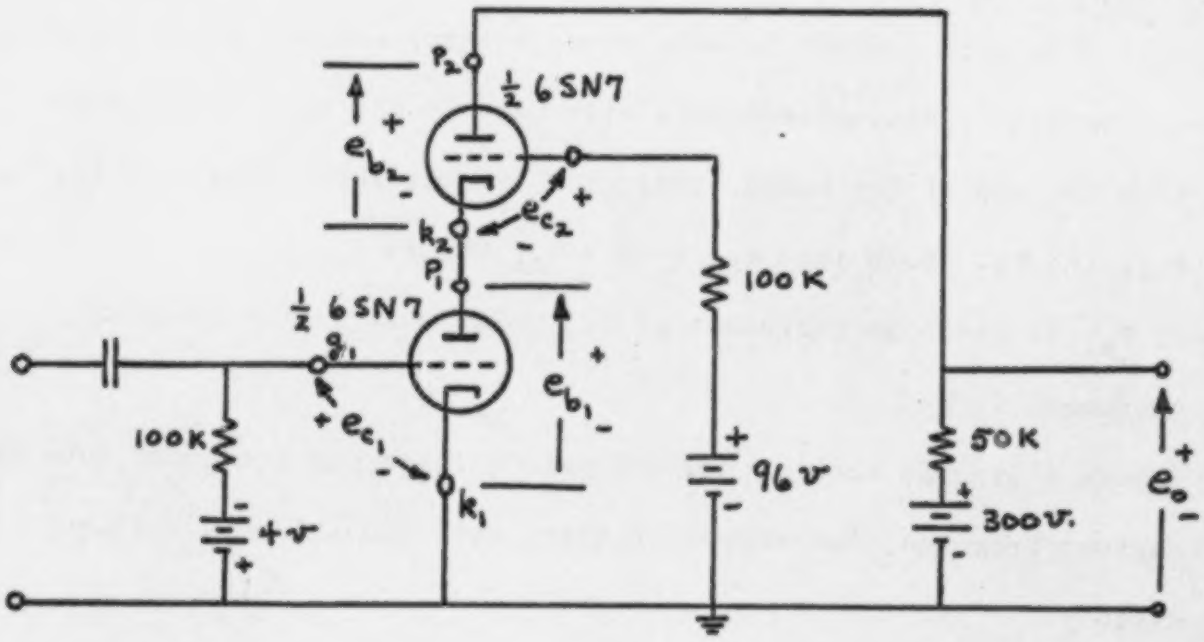
Construct the circuit of problem 6-5. Use a plate-load inductance value such that its reactance at 1000 rps will be the same numerical value as the original 50-kilohm plate-load resistance. All other components are identical to those specified in Problem 6-5.

1.) Plot the frequency response function A21 in decibels on a log-frequency scale over the interval 0.0001 to 10.0 kcps.

2.) Plot the amplitude and phase, and also the real and imaginary parts of the output admittance Y22 and the output impedance Z22 as a function of log-frequency over this same frequency interval.

Problem No. 6 - Angelo 5-13, page 152-153. Fig. 5-30 Piecewise Linear Analysis

Part A - Analytical Solution (from Text).


P2
½ 6SN7
+
e_{b_2}
-
k_2
e_{c_2}
+
-
P_1
½ 6SN7
g_1
+ e_{c_1}
-
k_1
+
e_{b_1}
-
100K
+v
100K
96v
50K
300V.
e_o
+
-

Taken from Angelo, p. 152, Fig. 5-13.

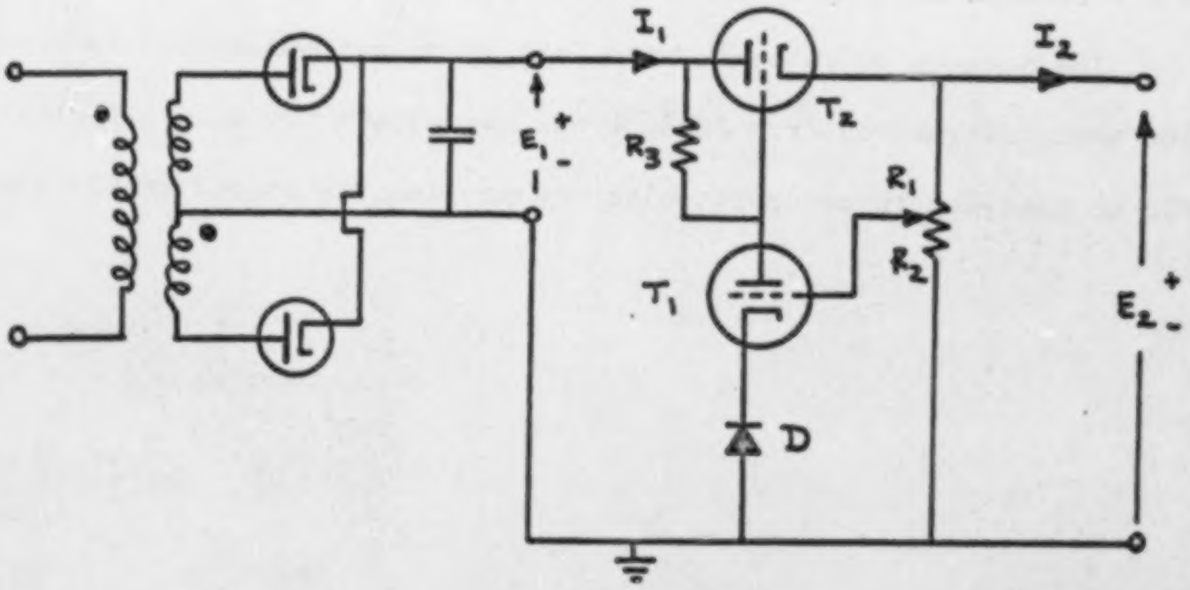

I_1
I_2
T_2
E_1
+
-
R_3
R_1
R_2
T_1
D
E_2
+
-

Fig. 5-22a, Voltage regulator.

The cascode amplifier shown in Fig. 5-31 is used in certain applications as a voltage amplifier. (For example, it is occasionally used in the voltage regulator of Fig. 5-22a in place of the one-tube amplifier consisting of T_1 and R_3 to provide more amplification and better regulation.) The grid current in each tube is zero, and the plate circuits can be represented by piecewise-models with $\mu = 20$ and $r_b = 10$ kilohoms.

a. With the aid of the model, determine the quiescent values of i_b, e_b, e_{b2}, and e_o. Note that $e_{c2} = 96 - e_{b1}$ volts.

b. If e_{c1} is given an increment of 0.1 volt, what is the resulting increment in e_o?

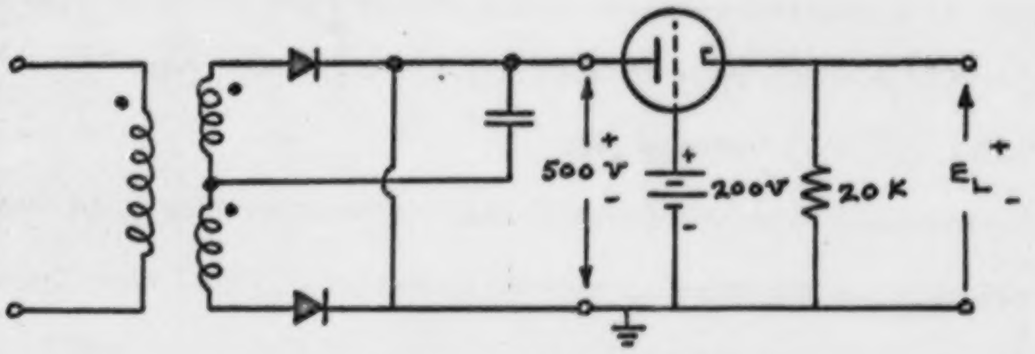
c. Sketch a diagram showing how the grid voltage for the upper tube can be derived from the plate-supply battery with the aid of a voltage divider.

Give the values of resistance required in the voltage divider if the total resistance is 100 kilohms.

Part B - JOBSHOP simulation (Given by Dr. Huggins).

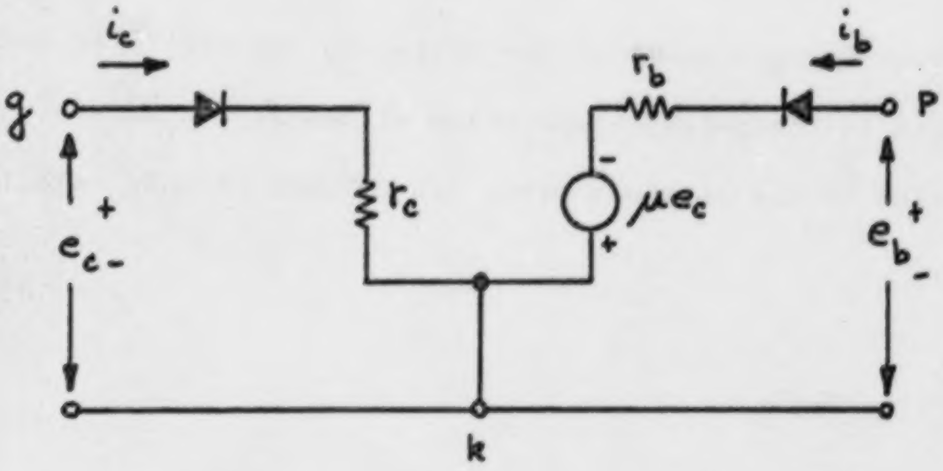
The methods of analysis were left up to the students. They were to decide what information from JOBSHOP was needed and how this information should be analyzed in order to solve the problem, as stated in the text.

Problem No. 7 - page 153-154, Fig. 5-13, Voltage Regulator Analysis.



Taken from Angelo, Fig. 5-32.

Part A - Analytical Solution (from Text).



Taken from Angelo, Fig. 5-16c.

The circuit of Fig. 5-32 is a full wave rectifier with a triode used as an elementary voltage regulator. The function of the regulator is, among other things, to hold the load voltage nearly constant in the face of changes in line voltage and to reduce the ripple voltage across the load. As an additional feature, the output voltage can be adjusted over a range of values by adjusting the voltage applied to the grid of the triode. (The performance of this elementary regulator should be compared with that of the more elaborate regulator analyzed in Example 5-5, page 146, Fig. 5-22a (see Problem No. 6 - Piecewise Linear Analysis).) The triode can be represented by a piecewise-linear model of the form shown in Fig. 5-16C, page 139, with $\mu = 60$, $r_b = 12$ kilohms, and $C_c = 500$ ohms.

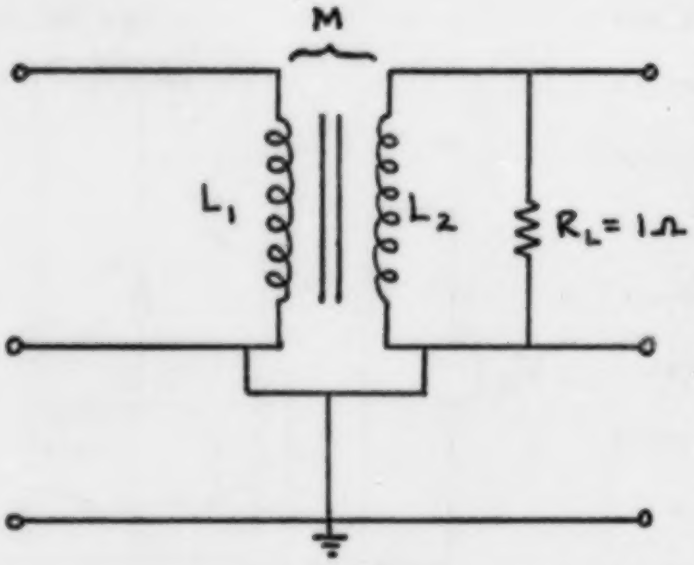
a. Determine the load voltage E_1.

Suggestion: For the first trial, assume that the grid current is zero, since this is the case in normal operation. Then, when the solution is completed, check the assumption

b. If the output voltage from the rectifier decreases by 10 per-cent, by what percentage does the load voltage change?

c. If the peak-to-peak value of the ripple in the rectifier output is 1 volt, what is the peak-to-peak value of the ripple across the load? The results of the previous parts can be used in this calculation if desired.

Problem No. 8 - Transformer Characteristics



$L_1 = 20$ h

$L_2 = 10$ h

$M = 14$ h

$$K^2 = \frac{M^2}{L_1 L_2} = 0.98$$

Transformer and Its Parameters to be used for Problem.

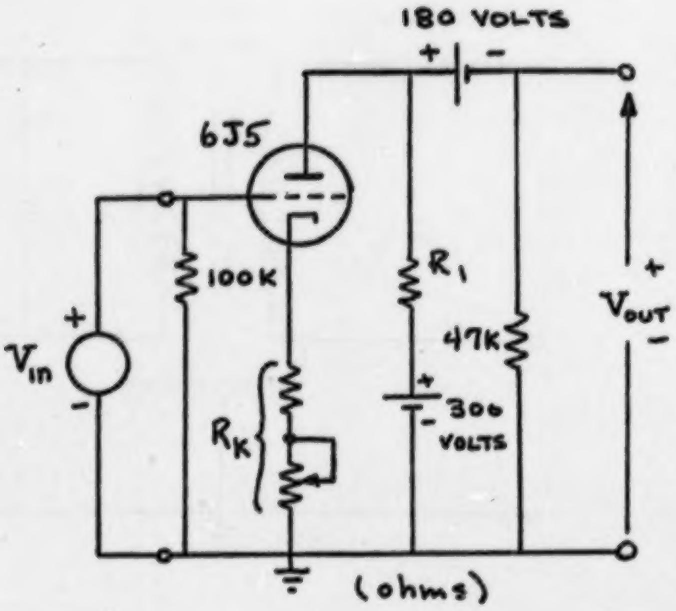
1.) Find expressions for Z11(s), A21(s), B21(s).

2.) Have JOBSHOP evaluate and plot these functions (AMP., GAIN, ANGL, REIM) on a logarithmic frequency scale over a range of $0.001 \leq \omega \leq 100.0$ radians/sec.

3.) Over what frequency range is $Z11(s) \simeq R1 \left(\frac{L1}{22}\right) = 2 + j0$

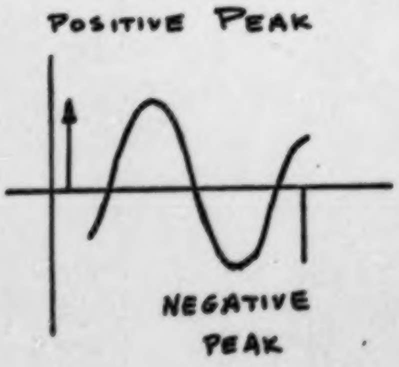
Problem No. 9 - Design 23 (D.C. Coupled Amplifier).

The circuit shown at the right is a direct-coupled amplifier in which the output voltage is nominally zero when the input voltage is zero. It is used to amplify direct voltages. The 180-volt battery is a small unit that conveniently subtracts 180-volts from the voltage at the plate to give the output signal.



1.) You are to determine the values of the resistors R_k and R_1 and the tolerance and power ratings of all resistors so that with no voltage applied to the input, the output voltage will surely be within ±5 volts of the ground voltage. That is, when $v_{in} = 0$, the output voltage will have a value somewhere within the range $-5 \leq v_{out} \leq +5$. Consider the battery voltages as accurately fixed at their specified values.

2.) This amplifier is used to amplify a sinusoidal voltage of the form $v_{in}(t) = E_{in} \cos \omega t$. As the input amplitude E_{in} is made larger, the amplitude V_{out} of the output signal will reach some maximum value beyond which the peak positive and negative changes are no longer equal. The resistors R_k and R_1 should be chosen so as to maximize this peak to peak voltage, subject to the condition

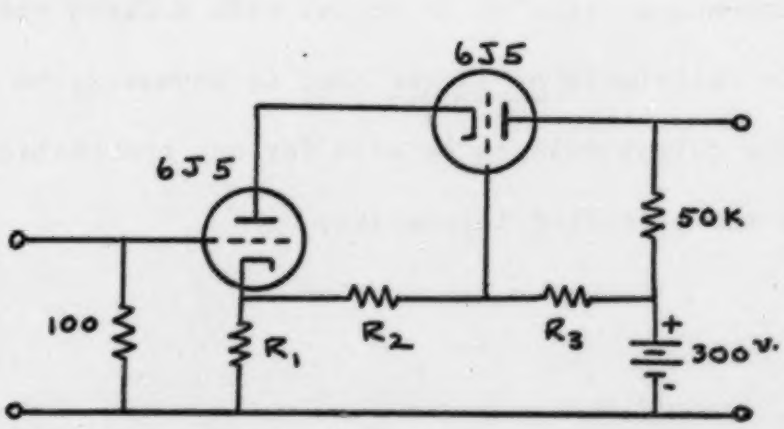


that values of the positive and negative peak variations should differ by no more than 5 percent.

3.) Use standard RETMA resistance values. The g_m and g_p parameters of the 6J5 tube are guaranteed to be within ± 10 percent of their nominal values and the μ is exactly 20. For the cathode resistor, use an adjustable wire-wound resistor in series with a fixed resistor, with the adjustable resistance no larger than is necessary to provide means for setting the output voltage to zero for any combination of parameter errors within the specified tolerances.

Problem No. 10 - Cascode Amplifier

Find the values of R_1, R_2, and R_3 such that d-c output voltage will be within the range 190-210 volts. Find tolerances on these resistors such that 10 units with the least total cost meeting this voltage specification can be built.

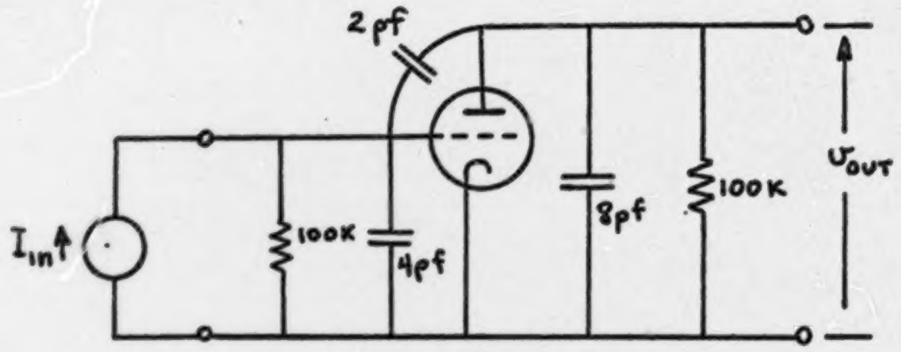


Cascode Amplifier

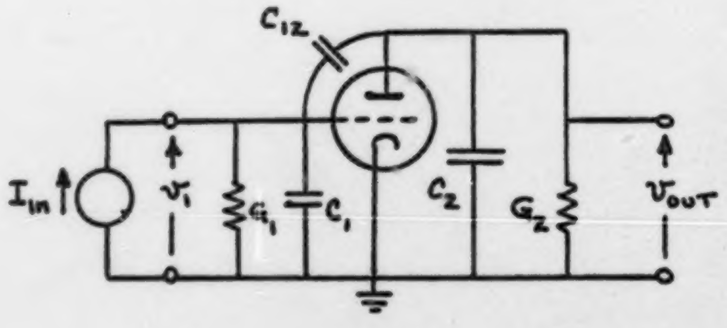
Problem No. 11 - Miller Effect

We have discussed the high-frequency response of the 12AX7 triode amplifier shown below. It has been shown that the high-frequency response is dominated by the Miller effect. The response was calculated by finding the effect of C_{12} on the input admittance. In this assignment, we consider another approach by finding the effect of C_{12} on the Norton equivalent at the output terminals.

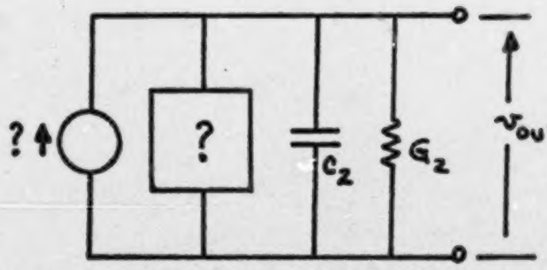
12AX7 $g_m = 1$ m mhos
$g_p = 0.01$ m mhos



a.) By eliminating the input node, find an equivalent circuit at the output terminals of this amplifier.



Amplifier Circuit



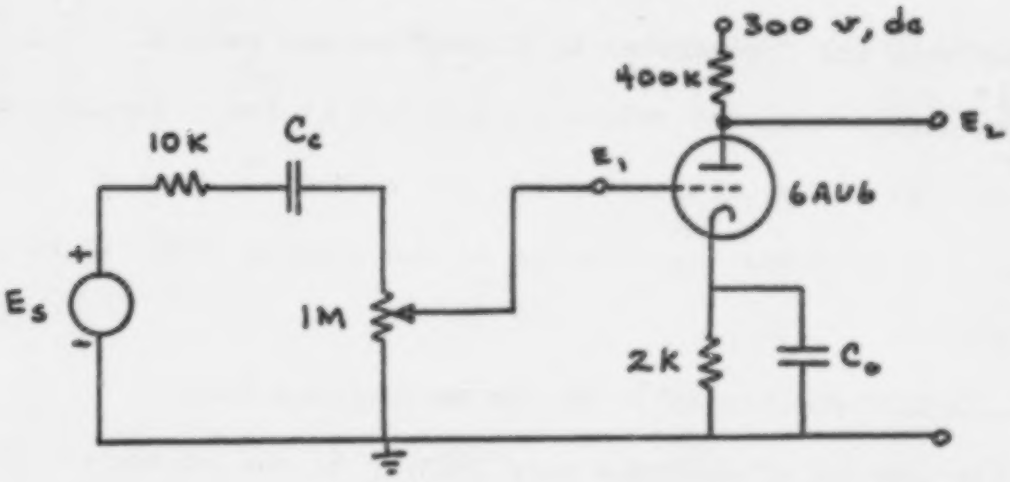
Norton Equivalent

b.) Use this equivalent circuit to estimate the 3-db bandwidth and the amplification of the amplifier. Compare this with the results obtained by use of the equivalent-input-circuit method.

c.) If an additional load, consisting of a 10-μfd capacitance is connected across the output terminals, what would be the new 3-db bandwidth? Use JOBSHOP to build and test the circuits of part b) and c).

d.) Explain the significance of the second sentence of the caption to Fig. 16-16 on page 466 of the text in the light of your work.

Problem No. 12 - Angelo 16-15, page 484-485, Fig. 16-24



Taken from Angelo, Fig. 16-24.

Part

The triode amplifier shown in Fig. 16-24 is provided with a 1-megohm potentiometer to serve as a volume control. The effect of the volume control on the high-frequency characteristics is to be examined. The incremental parameters for the tube are $\mu = 100$ and $r_p = 80$ kilohms; the parasitic capacitances of the tube and wiring are $C_1 = C_2 = 5$ $\mu\mu f$ and 3 $\mu\mu f$; the coupling and bypass capacitors act as short circuits at all frequencies of interest.

a. The input to the triode can be represented by an equivalent circuit of the form as shown in Fig. 16-16. Determine the values of the parameters in this circuit.

b. Sketch and dimension the asymptotes for the high-frequency amplitude characteristics of the voltage ratio E_1/E_s for the condition that the volume control is set for maximum output voltage. For this calculation the resistance R can be treated as a short circuit. Give amplitudes in decibels and frequencies in kilocycles per second.

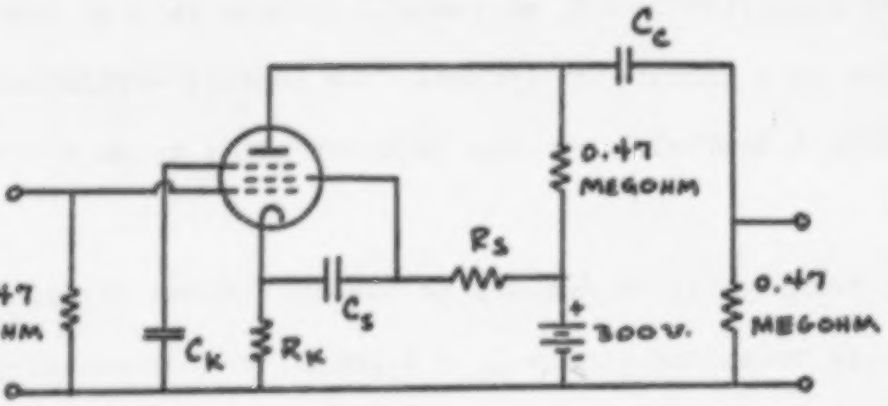
c. Repeat part b with the volume control set at its mid-point (that is, set so that the potentiometer has 500 kilohms on each of the slides).

d. Discuss briefly the significance of the results obtained in parts b and c.

Part B - JOBSHOP simulation (Given by Dr. Huggins.)

The methods of analysis were left up to the students. They were to decide what information should be analyzed in order to solve the problem as stated in the text.

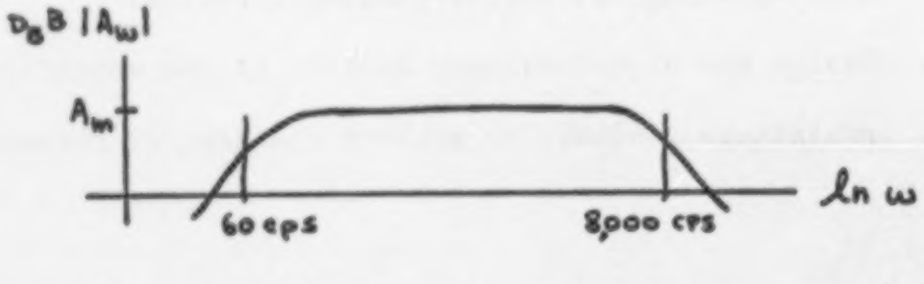
Problem No. 13 - Single Stage Pentode Bandpass Amplifier Design



A). Determine values of R_s, R_k to provide a good operating point. (Note that dynamic load line differs from static line).

B). Find values of C_k, C_s, and C_c so the low-frequency 3-db point of the voltage amplification will occur at 60 cps.

C). It is desired to limit the high-frequency response of the amplifier so that the upper-3-db point occurs at 8,000 cps.



Find the value of the capacitance C_o that should be connected across the output to achieve the desired roll-off at high frequencies.

D). Use JOBSHOP to verify your design.

Problem No. 14 - Low Pass Video Amplifier Design

A video amplifier having an overall voltage gain of 100 decibels is required for use in a television system. The overall amplification should be flat to within 3 decibels over the band extending up to 4 Megacycles per second.

For uniformity, it is decided to use 6SJ7 tubes throughout, with the grid-to-plate transconductance $g_m = 2$ mmhos, the screen-to-plate transconductance $g_s = 0.1$ mmhos, and the screen-to-plate current ratio $\rho = 0.25$. The plate conductance g_p may be neglected.

The equivalent grid capacitance $C_g = 8\ \mu\mu$fd and the plate capacitance $C_p = 7\ \mu\mu$fd. The plate-to-grid capacitance is negligible.

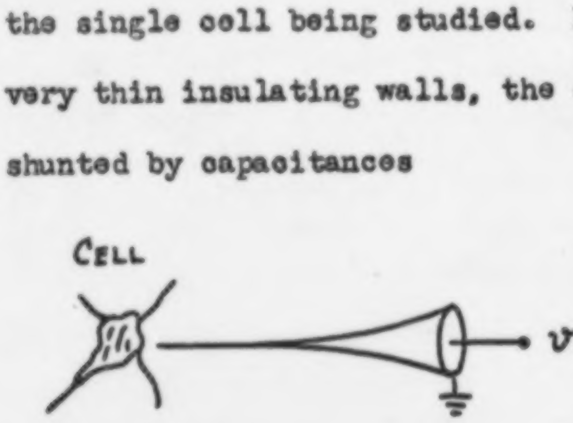
1). How many stages of amplification will be required for a Butterworth response?

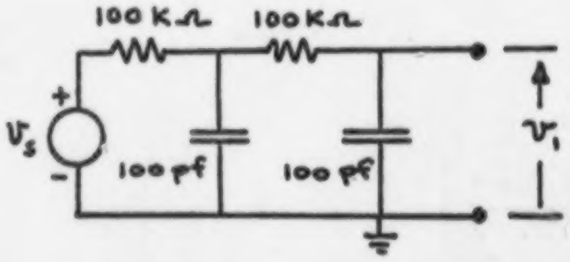
2). Discuss possible alternatives using resistance feedback, shunt-peaking and series-peaking circuits.

3). Design the high-frequency aspects of the amplifier using only resistance feedback to achieve the desired overall response.

Problem No. 15 - Final Design Problem

In studying the functioning of the nervous system, the small voltages or action potentials produced when a nerve cell "fires" are often measured by using a microelectrode. This microelectrode is insulated except for its tiny tip which may be inserted into the nerve fiber next to the single cell being studied. Because of its extremely small size and very thin insulating walls, the electrode acts as a high series resistance shunted by capacitances

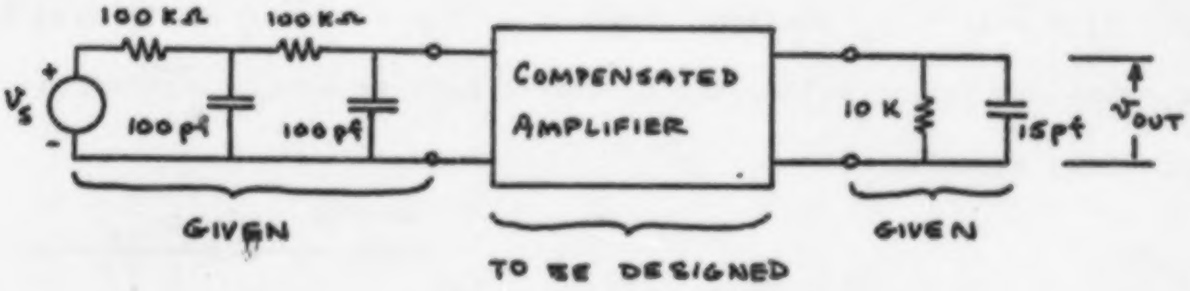


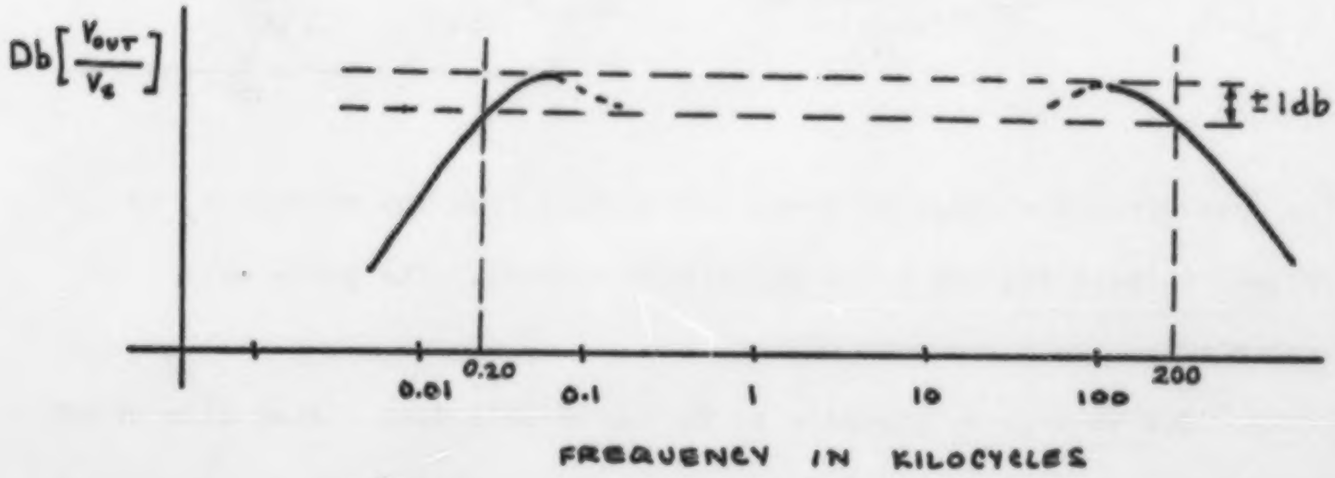


The open-circuit voltage v_1 therefore differs from the voltage v_s by virtue of these resistive and capacitive effects. The probe acts essentially like a low-pass filter.

The voltage v_s produced by the nerve cell upon firing is a brief "spike" or pulse of very brief duration. The amplitude of v_s is about 1 millivolt. It is desired to amplify this small signal with a wide-band amplifier so as to permit a study of the wave-shape of a single spike. It has already been determined that if the amplifier has an upper cut-off frequency of 200 kilocycles per second, the fine detail will be adequately reproduced. The amplification must be sufficient so that a 1-millivolt spike, v_s, will produce an output signal of at least 10 volts peak amplitude, across a 10 kilohm load having a stray shunt capacitance of 15 pf.

The amplifier is to compensate for the low-pass filter characteristics of the microelectrode. It should also amplify uniformly down to 20 cycles per second or less so as to minimize the wave distortion of slowly varying components. These requirements are summarized in the following diagram.


100 KΩ
100 KΩ
V_s
+
-
100 pf
100 pf
COMPENSATED AMPLIFIER
10 K
15 pf
v_{OUT}
GIVEN
TO BE DESIGNED
GIVEN

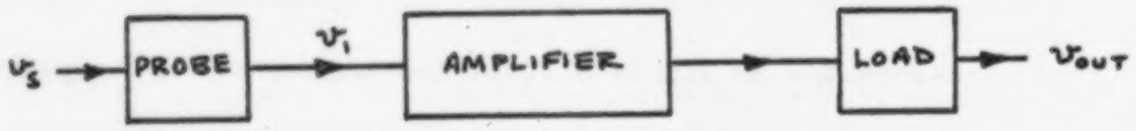


The amplification $\frac{V_{out}}{V_s}$ should be adequate so that a 1-millivolt signal v_s will appear as a 10-volt signal, v_{out}, across the load. Notice that V_s is not V_1, the voltage at the input terminals of the amplifier. The overall response, including that of the microelectrode, is to be flat to contain ± 1 dbs over the frequency band from 20 cps to 200 kilo cps.

It is suggested that 6SJ7 tubes be used with appropriate values for their input and output stage capacitances. Also, since a 300-volt power supply is readily available, the circuits should be designed to operate from this supply.

Outline of Solution

The overall system consists of three components: the source probe, the amplifier, and the load.



Because the load is a parallel combination, it can easily be incorporated into the design of the last stage of the amplifier. The probe, however, requires special consideration. The following steps are suggested.

1. Estimate transfer function of probe to express v_1 in terms of v_s. (Take input loading of amplifier into account.)
2. Decide on some equalizing scheme to compensate for the undesired poles of the probe. (Probably use shunt peaking circuits in amplifier stages.)
3. From consideration of the compensation circuits used, estimate number of stages required to achieve 200 kcps Bandwidth (Use Butterworth design initially to estimate gain requirements.)
4. Settle on final pole distribution to achieve ± 1db high-frequency response and design high-frequency coupling circuits.
5. Choose D.C. operating characteristics and compute cathode and screen resistors and plate supply decoupling resistors.

6. Work out low-frequency design - determine capacitances, screen-bypass capacitances and a cut-off to achieve 20 cps low-frequency.
7. Test design on JOBSHOP. (Simulate probe as well as load.) Measure also open-circuit amplification $\frac{V_{out}}{V_1}$ when input and output circuits are removed from amplifier. It will be desireable to simulate first the high-frequency aspects of the circuit on JOBSHOP (by treating all by-pass capacitors as short-circuits), and then to treat only the low-frequency aspects (to check screen-dropping resistors and cathode-bias resistors and the adequacy of their bypassing capacitors. Here, small inductances will behave as short-circuits).

II.B.2 DESIGN PROBLEMS
IN SUMMER SESSIONS.
STUDENTS VS. CONSULTANTS
1. D-C COUPLED AMPLIFIER

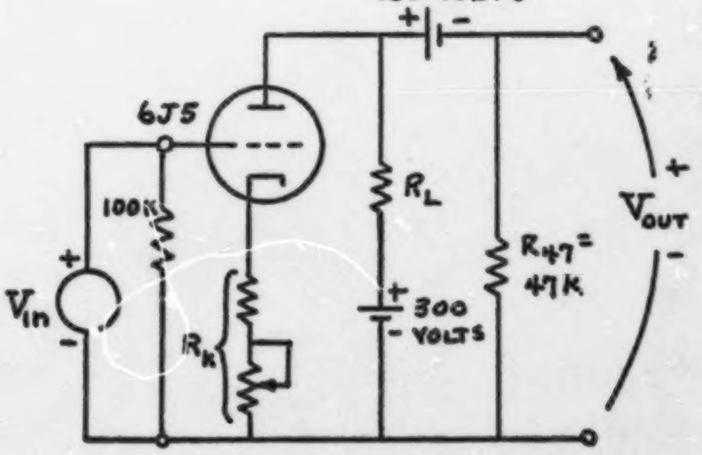
by RICHARD SABAT

I. Purpose:

The purpose of this report will be to study the similarities and differences in the approaches of the students and experienced consultant engineers in solving Design Problem No. 23 of the JOBSHOP research program. The first part of the report is a statement of the problem as presented to both students and consultants. The second and third parts are concerned with the students' and consultants' approaches, respectively. The fourth and final part is devoted to comparison of the two approaches and conclusions reached from this comparison. This comparison will be qualitative rather than quantitative. That is, such items as actual design values (value of circuit elements, tolerances, etc.) decided upon will not be emphasized. What will be stressed are similarities and differences of the consultants' analytical methods and the students' analytical methods, plus the role played by JOBSHOP in solving the problem.

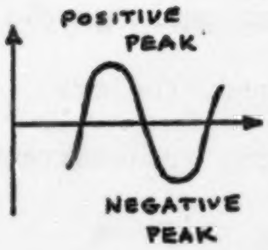
II. Problem:

The circuit shown at the right is a direct coupled amplifier in which the output voltage is zero. It is used to amplify direct voltages. The 180 volt battery is a small unit that conveniently subtracts 180-volts from the voltage at the plate to give the output signal.



1) You are to determine the values of the resistors R_k and R_L and the tolerance and power ratings of all resistors so that with no voltage applied to the input, the output voltage will surely be within ±5 volts of the ground voltage. That is, when $v_{in} = 0$, the output voltage will have a value somewhere within the range $-5 \leq v_{out} \leq +5$. Consider the battery voltages as accurately fixed at their specified values.

2) This amplifier is used to amplify a sinusoidal voltage of the form $v_{in}(t) = E_{in} \cos \omega t$. As the input amplitude E_{in} is made larger, the amplitude v_{out} of the output signal will reach some maximum value beyond which the peak positive and negative changes are no longer equal. The resistors R_k and R_L should be chosen so as to maximize this peak to peak voltage, subject to the condition that values of the positive and negative peak variations should differ by no more than 5 percent.



3) Use standard RETMA resistance values. The g_m and g_p parameters of the 6J5 tube are guaranteed to be within ±10 percent of their nominal values and the μ is exactly 20. For the cathode resistor, use an adjustable wire-wound resistor in series with a fixed resistor, with the adjustable resistance no larger than is necessary to provide means for setting the output voltage to zero for any combination of parameter errors within the specified

tolerances.

III. Students' Approach:

A. Overview of the Analysis and Design

The first thing which all the students did was to establish criteria for the selection of a quiescent point. The criteria were based partly on the design specifications and partly on experience obtained in solving previous design problems. The criteria used by the students were (1) The quiescent plate voltage should be 180 volts minus a small drop across the cathode resistor (on the order of 5 volts). (2) The quiescent point should be located in the most linear region of the tube characteristics so that one could get maximum voltage swing on the grid and minimum distortion of the output signal (no greater than 5% difference between the positive and negative peak values of the output signal). (3) The quiescent point should be located so that when maximum grid voltage swing was obtained, the grid would not become more positive than zero volts, thus preventing grid current to be drawn. (4) The plate dissipation should not be greater than the maximum power rating as specified on the tube characteristics. If possible, plate dissipation should be only one-half of the maximum power rating.

The graphical method employed by the students in locating the Q-point is illustrated in Figure III-1. (One should note that the curves are by no means accurate and are for illustrative purposes only.) The students proceeded by finding the point where all load lines crossed at the coordinate

$$(e_b', i_b')$$

where

$$e_b' = eb\big|_{ib = 0} \quad \text{and} \quad ib' = ib\big|_{eb = 0}$$

These values were obtained by solving the equations describing the plate

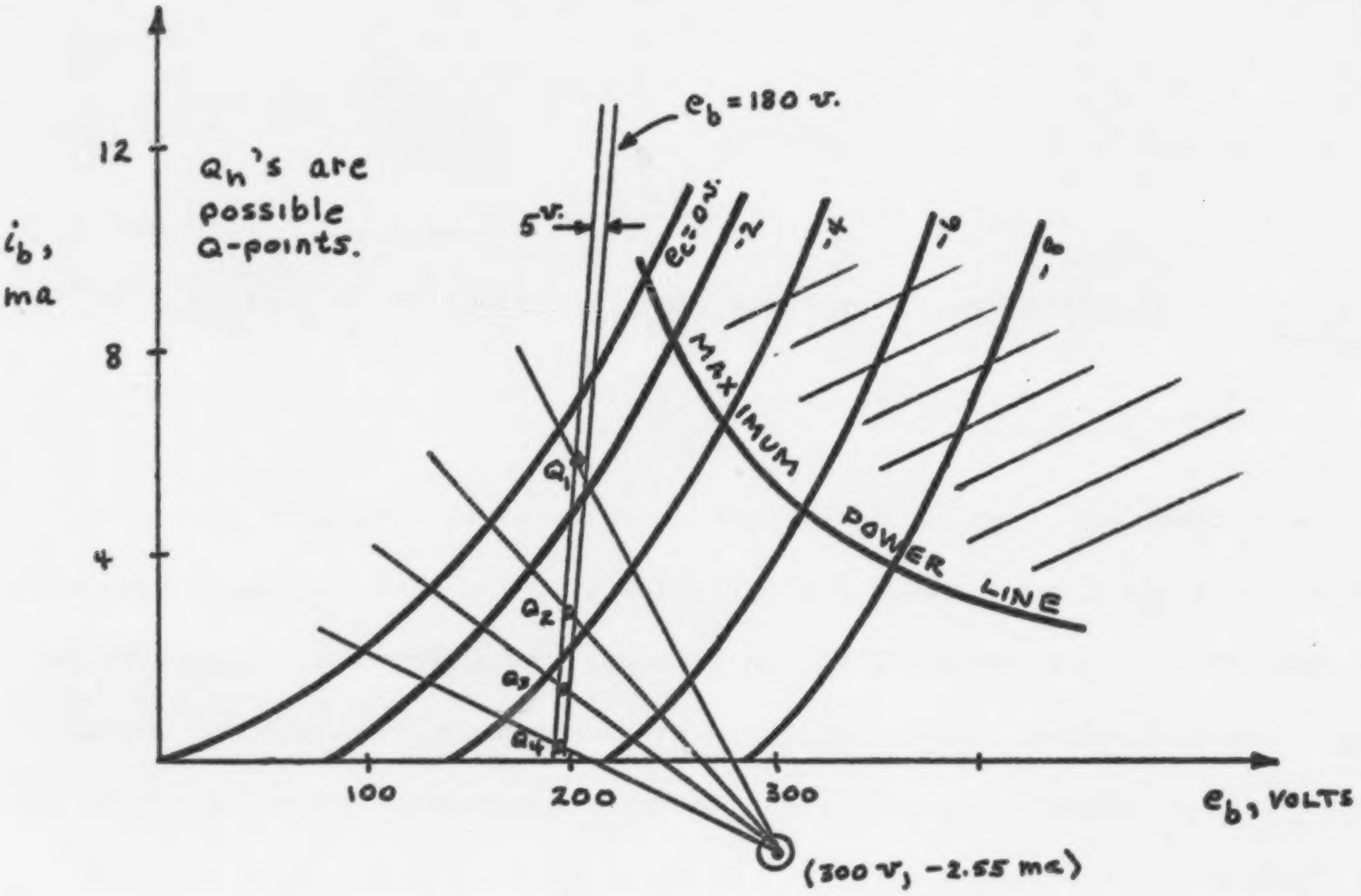


Fig. III-1. Illustrative 6J5-Static Plate Characteristics

circuit. Then several load lines were swung around this point. This gave a series of possible Q-points, on or within 5 volts of the intersection of the e_b = 180v line and the various load lines. Then the previous criteria were used to select the final Q-point.

The next step was to calculate the nominal resistance values of R_L and R_k to give the desired output (0 volts $\pm$5 volts output signal for no applied input signal) under operating conditions discussed previously. There were several methods employed by the students in calculating these resistance values. Using the original (given circuit), the cathode resistance was calculated by

$$R_k = \frac{ec|_Q}{ib|_Q}$$

The load resistance was calculated by

$$R_L = \frac{300\text{-}180}{ib|_Q}$$

or by setting the slope of the final load line equal to

$$-\frac{1}{\frac{R_L 47}{RL + 47}} .$$

Some students used various equivalent circuits of the original circuit to find the resistance values. The replacement of the cathode-loaded tube with a tube with no cathode resistor was a common transformation. Here, the new g_m (tube trans-conductance) and g_p (plate admittance) were altered to take into account cathode degeneration. Another common transformation was to use a Thevinin equivalent circuit for the plate-load circuit. Some students also used the linear-incremental model of the vacuum tube or variations of the basic model. These, the most common transformations are shown in Figs. III-2, III-3, and III-4 respectively.

Although there were many variations of these transformations, these are the three basic ones most often used. They illustrate the types of transformations tried. After the students had made these transformations they used various network theorems to find the values of R_L and R_k.

The tube parameters g_m and g_p were not determined by graphical methods and the values given ($g_m = 2.0$ m$\mho$ and $g_p - 0.1$ m$\mho$) were used.

The next part of the analysis was the determination of the tolerances. One of the most frequently-used methods was logarithmic differentiation. That is, using node-pair equations or other network equations on the original circuit or the equivalent circuits, the students were able to write a transfer function

$$\frac{v_{out}}{v_{in}} = f_1(g_m, g_p, R_L, R_{47}, R_k)$$

Then by using logarithmic differentiation, a function

$$\frac{\Delta v_{out}}{v_{out}} = \frac{5}{180} = f_2(g_m, g_p, R_L, R_{47}, R_k)$$

could be obtained. By holding all but one parameter at zero tolerance, one can obtain a value of $\frac{\Delta x}{x}$ to give the maximum tolerance on any one parameter, $\underline{x}$.

A second method, single parameter variation, was also used. With all parameters fixed but one, the student would vary this parameter and find the corresponding value of v_{out} . Then the student had v_{out} = f(variable parameter) which could either be tabulated or graphed. The maximum change in the parameter is the value for which

$$v_{out} = 0 \pm 5 \text{ volts}$$

for $v_{in} = 0$.

When the tolerances were finally found, the variable potentiometer to be connected to R_L to make $v_{out} = 0$ when $v_{in} = 0$ was then determined. This was done by making it equal the variation in R_k needed if all parameters varied to their worst case values. The tolerance on the potentiometer was assumed equal to 0.

The final step in the analytical work, determination of the maximum power ratings, was easily obtained from the definition of power (P = IE). Tolerance considerations were used to determine the maximum power dissipated when the parameters varied over their possible ranges. The maximum dissipation in any one parameter was calculated.

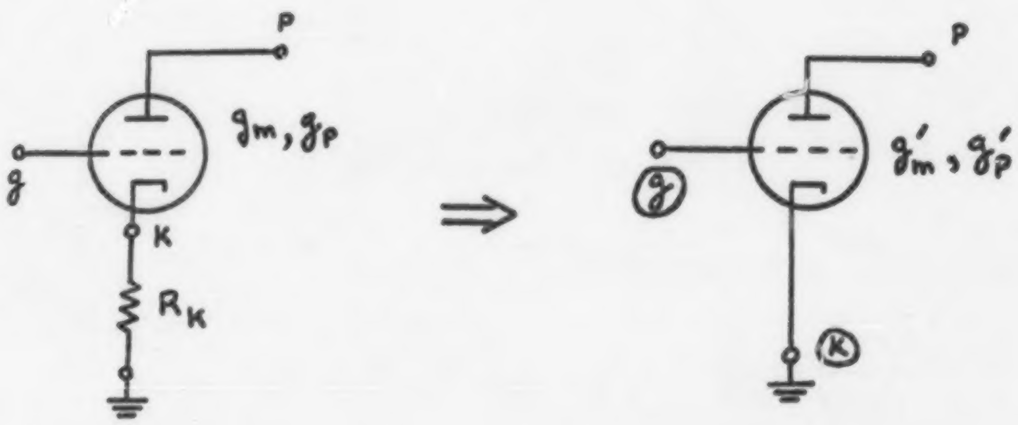
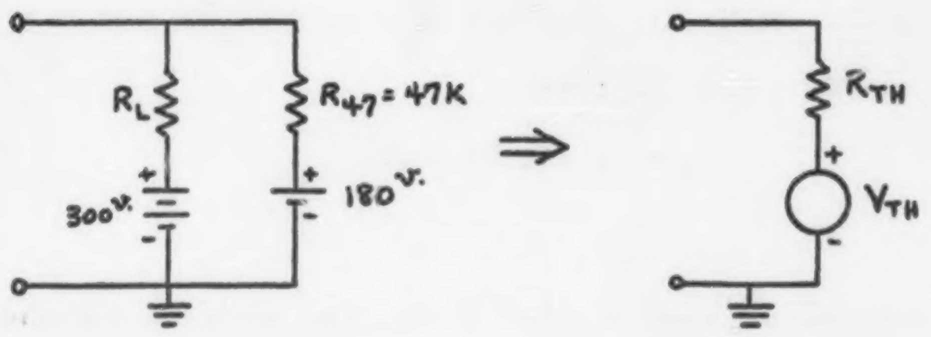

P
g
g_m, g_p
K
R_K
⇒
P
g
g'_m, g'_p
K

Fig. III-2. Equivalent Tube Transformation

where

$$g'_m = g_m \frac{1}{1 + (g_m+g_p)R_k}$$

$$g'_p = g_p \frac{1}{1 + (g_m+g_p)R_k}$$


R_L
$R_{47} = 47K$
$300^{v.}$
$180^{v.}$
+
-
⇒
R_{TH}
V_{TH}
+
-

$$R_{TH} = \frac{47 R_L}{R_L + 47}$$

$$V_{TH} = 300 - \frac{120 R_L}{R_L + 47}$$

Fig. III-3. Thevinin Equivalent of Plate Load Circuit

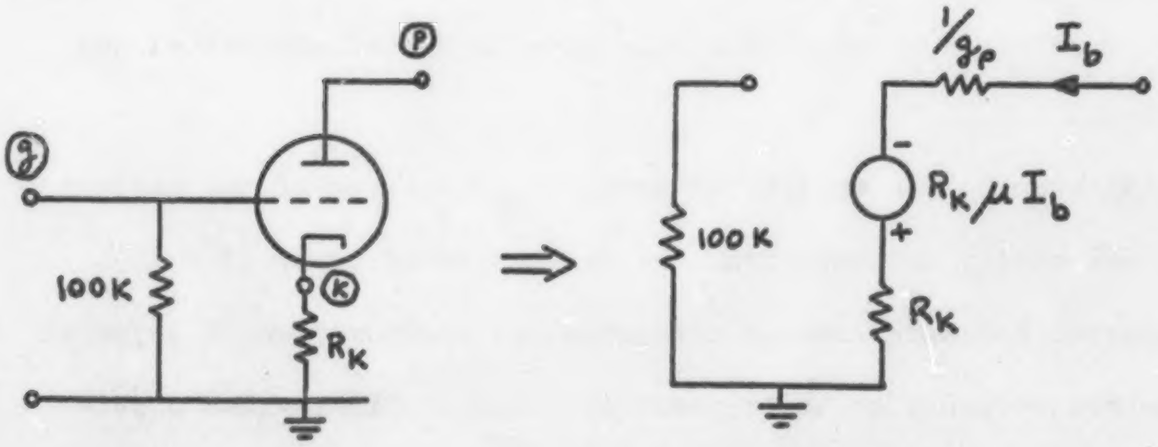

P
g
100K
K
R_K
⇒
$1/g_p$
I_b
100K
-
$R_K \mu I_b$
+
R_K

Fig. III-4. Linear Incremental Model

B. JOBSHOP Analysis

The majority of the students used JOBSHOP primarily to determine the nominal values and tolerances of the parameters. In conducting their analysis the students used mostly one very important feature of the program. This feature is the ability to augment or vary the tolerances and nominal values of one or more parameters.

There were several ways in which these parameters were varied in order to study the effect on the output voltage. Some students tried multi-parameter variation. That is, they varied two, three, four and in some cases five parameters (i.e. R_k, R_L, g_m, g_p, R_{47}) in order to study the effect on the output voltage. From a survey of students' work on this problem, it is very evident that when more than two parameters were varied simultaneously, the students had difficulty evaluating the data. This statement is based on the fact that not many students indicated in their write-ups of the problem that they had used the JOBSHOP results to make qualitative or quantitative conclusions concerning multi-parameter variations. In fact, the analysis of the data when just two parameters were varied simultaneously was quite challenging. Nevertheless some students were very successful in this type of approach. A description of the primary ways in which students used single and multi-parameter variation to solve the problem is given below.

In order to make the JOBSHOP simulation closer to the real-world problem, most of the students added an offset current generator (between cathode and plate) to the circuit. The value of this generator was determined by a method shown in class (use of the tube parameters, g_m, g_p, and the quiescent conditions). This value should remain a constant unless the tube parameters change or the quiescent point changes. Even so the generator is a function of the tube and its parameters. Most students realized this, but some thought the parameter could be varied in order to meet the design specifications, by augmenting the value on JOBSHOP. This was a fairly common misconception and use of the program corrected this mistake.

The most common dual component variations (also the ones for which the students could best analyze the data) were those of varying g_m and g_p simultaneously, and varying R_k and the cathode-potentiometer (call it R_k) simultaneously.

Assuming $$u = g_m/g_p$$ was a constant, most students concluded (after analyzing the data) that variation of g_m and variation of g_p had very similar effects on the output.

By varying R_k and R_k' together some students were able to determine the range on R_k that was needed in order for the output to be zero when the input was zero. That is, they found out how big R_k' had to be in order that the output could be set to zero, even if R_k took on its worst case values. Some students found a more successful method was to fix R_k at its worst-case values and to vary R_k' until zero output was obtained. In some instances the other parameters were fixed at their worst-case values too.

The most successful method and the method used by the majority of the students was to hold all parameters constant except one, which was varied. Then the voltage at the plate was plotted as a function of the parameter. The parameter value for which this voltage was 180 volts (equivalent to having the output voltage zero) was taken as the nominal value of the parameter. The values of the parameter for which the voltage was 180 ±5 volts were taken as the maximum variation of the parameter. From these measurements the maximum tolerance on each parameter with the tolerances of the other parameters equal to zero could be found. This is shown in Fig. III-5 below.

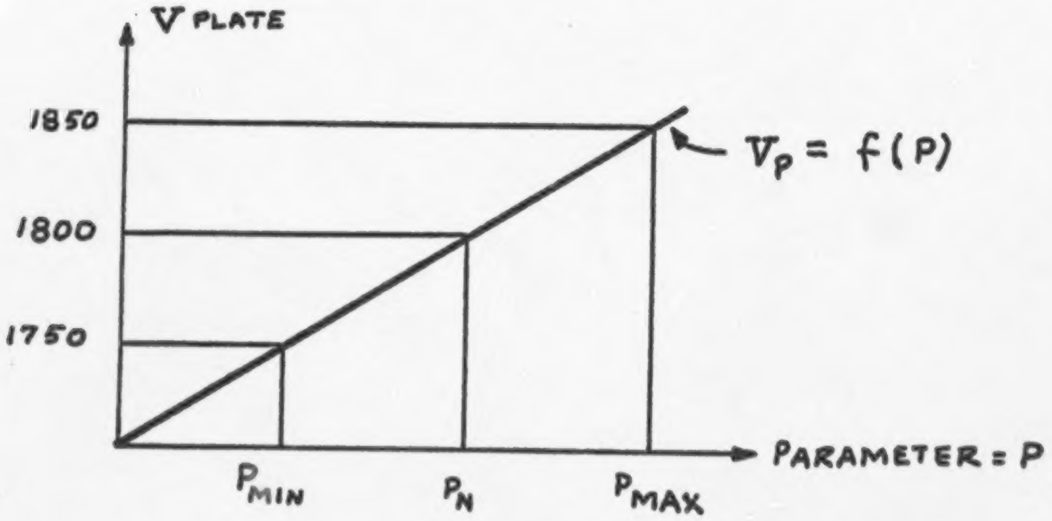


Fig. III-5. Graphical Solution of Tolerance Values

PN = Nominal Value of Parameter

$$\text{Tolerance } (\%) = \frac{PN - PMIN}{PN} \times 100 = \frac{PMAX - PN}{PN} \times 100$$

The parameter and tolerance investigations were the principal uses made of JOBSHOP for this problem. One final use of the program should be described, however, since it shows a misconception on the part of several students. Some students attempted to analyze the distortion by varying the input voltage in a sinusoidal manner using augmentation cards (i.e. putting in voltages of 0, 0.5, 0.707, 1, -0.5, -0.707, -1). Then, by observing the output voltage they hoped to find out if there was an equal amplification of positive and negative input signals of the same absolute magnitude (constitutes distortion). The students, however, failed to realize that on JOBSHOP a vacuum tube is linear and there will be no distortion. (All elements are modelled linearly in JOBSHOP.)

This concludes the analysis of the students' approach to the problem.

IV. Consultants' Approach:

A. Overview of the Analysis and Design

Like most of the students who worked on this problem, the consultants first determined criteria for the selection of a quiescent operating point (Q-point). Below appears a list of criteria used by the majority of consultants.

1) **The quiescent point should be located in a linear region of the characteristic curves of the 6J5 triode, so there will be minimum distortion of the output signal.**
2) **The quiescent point should be located so that there will be maximum voltage swing on the grid without going into the positive grid region and causing grid current to flow (thus destroying the tube).**
3) **The quiescent operating point should not be too close to the maximum power region of operation.**
4) **The quiescent plate voltage should be approximately 180 volts minus a small drop across the cathode resistor.**
5) **The cathode resistance should be large enough so that cathode degeneration will ensure stabilization of the amplifier.**

The next step in the analysis of the consultants was the selection of an operating point, based on the above criteria. To find the operating point the engineers used various equivalent circuits and network theorems and so wrote loop and nodal equations which related the various parameters of the system (eg. resistances, currents, and voltages). The next step was then

either to solve the analytical expressions and/or to use graphical methods to find the Q-point.

Because the aim of this report is to study the techniques of analysis, the great mass of equations typical of the consultants' work on this problem, will not be included. Rather we will try to summarize the basic steps of analysis. We will start by showing the equivalent circuits used by the majority of the engineers. Below appears typical circuits which, along with the original circuit, were used to obtain analytical expressions to describe the system.

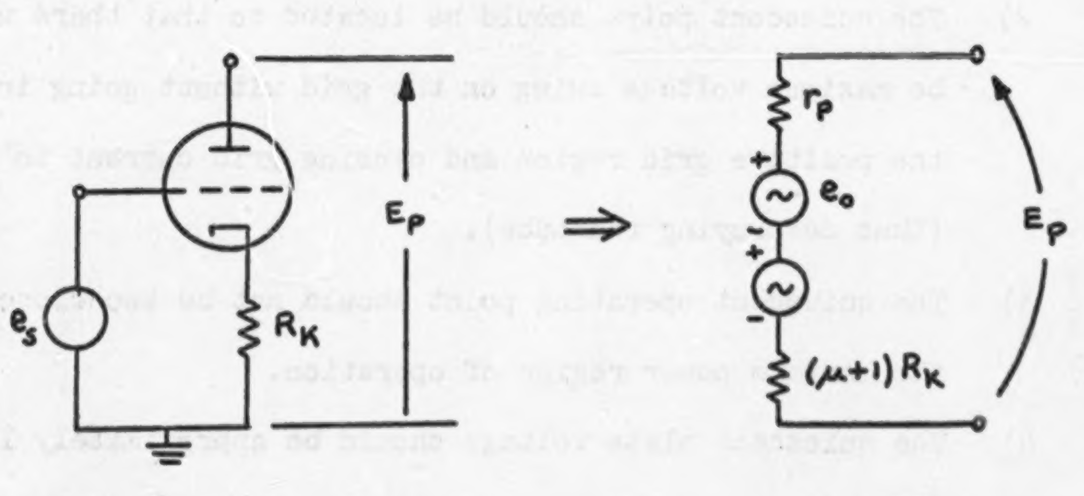


Fig. IV-1. Linear Equivalent Circuit of a Vacuum Tube

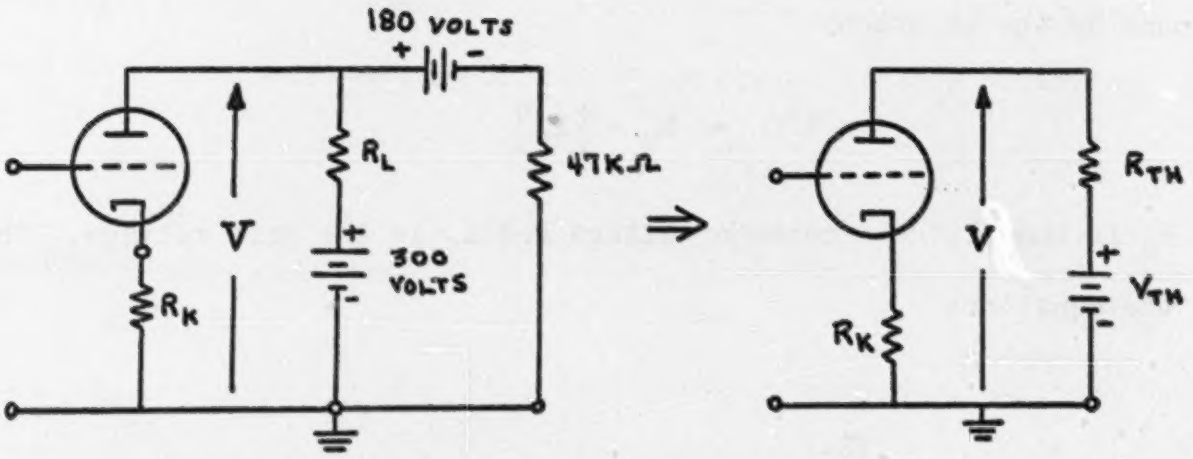


Fig. IV-2. Thevinin Equivalent Circuit of the

Plate Supply and Load Circuit

where

$$R_{Th} = \frac{R_L 47}{R_L + 47}$$

and

$$V_{Th} = 300 - \frac{120R_L}{R_L + 47}$$

In finding the Q-point and the nominal values of R_L and R_k, the engineers used several techniques. One method was exactly the same as that used by the majority of the students. This technique is described in section II, pages 3, 4, 5, paragraphs 1-2. There were some slight variations in this technique, but the method used by both students and consultants was basically the same.

Other methods used by the consultants to find the Q-point and resistance values R_L and R_k, are described on the next page.

1) One method was to find the locus of all Q-points which satisfy the condition that $v_{OUT} \equiv 0$ when $v_{IN} \equiv 0$. With this constraint the locus was found by the equation:

$$180 = E_b + |E_c|$$

where E_b is the plate-to-cathode voltage and E_c is the grid voltage. Then using the equations

$$R_k = \frac{(E_c)_Q}{(I_b)_Q} \quad \text{and} \quad R_L = \frac{300 - 120}{(I_b)_Q} = \frac{180}{(I_b)_Q}$$

several trial load lines are passed through these possible Q-points. The slope is

$$S = -\frac{R_L 47}{R_L + 47}$$

and the final Q-point and resistance values were determined using the criteria for the locating of a good Q-point as stated earlier. This is illustrated in Fig. IV-3.

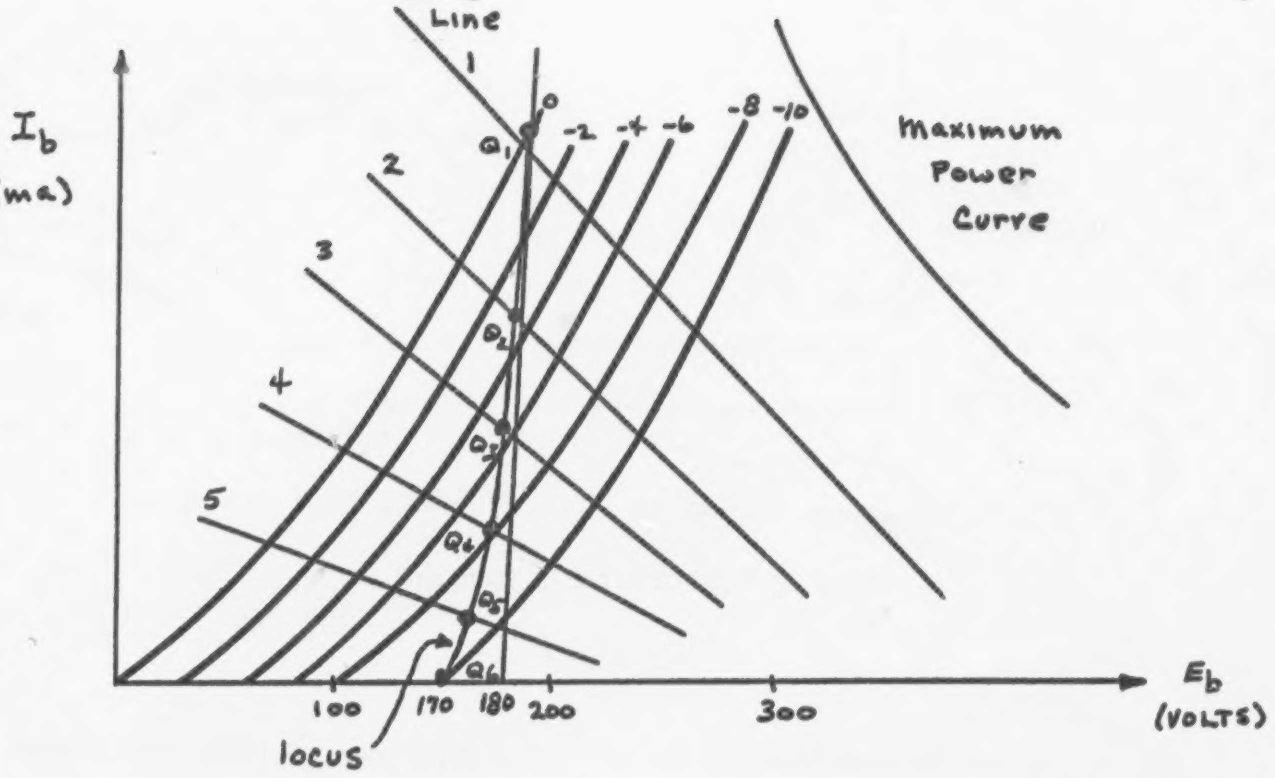
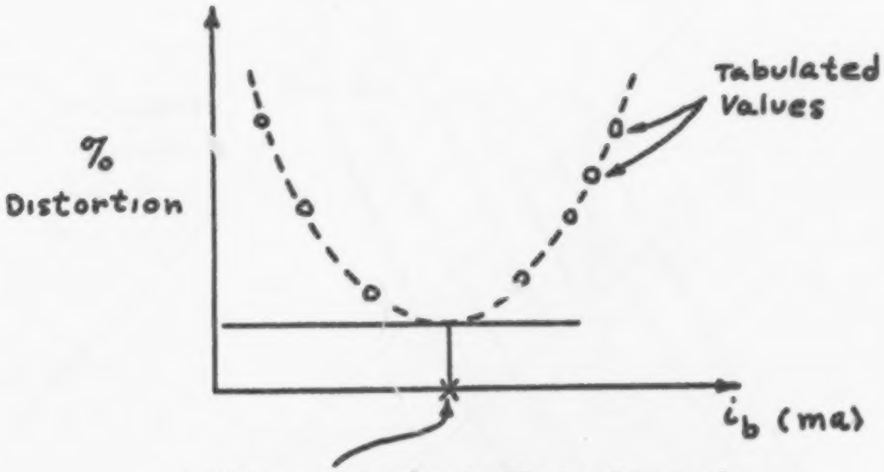

Load Line
1
I_b
(ma)
0
-2
-4
-6
-8
-10
Maximum Power Curve
Q_1
2
3
Q_2
4
Q_3
5
Q_4
Q_5
Q_6
100
170
180
200
300
E_b
(VOLTS)
locus

Fig. IV-3.

2) Several consultants used graphical methods to find the distortion of the output signal to locate a good Q-point, maximum voltage input, and resistance values. (Other criteria for the selection of the Q-point were also used.) One consultant tabulated the % distortion for various plate currents. Then these values were plotted and an optimum Q-point was selected. An illustrative plot is shown on the following page.



Optimum Quiescent Plate Current

(Using Distortion Criteria)

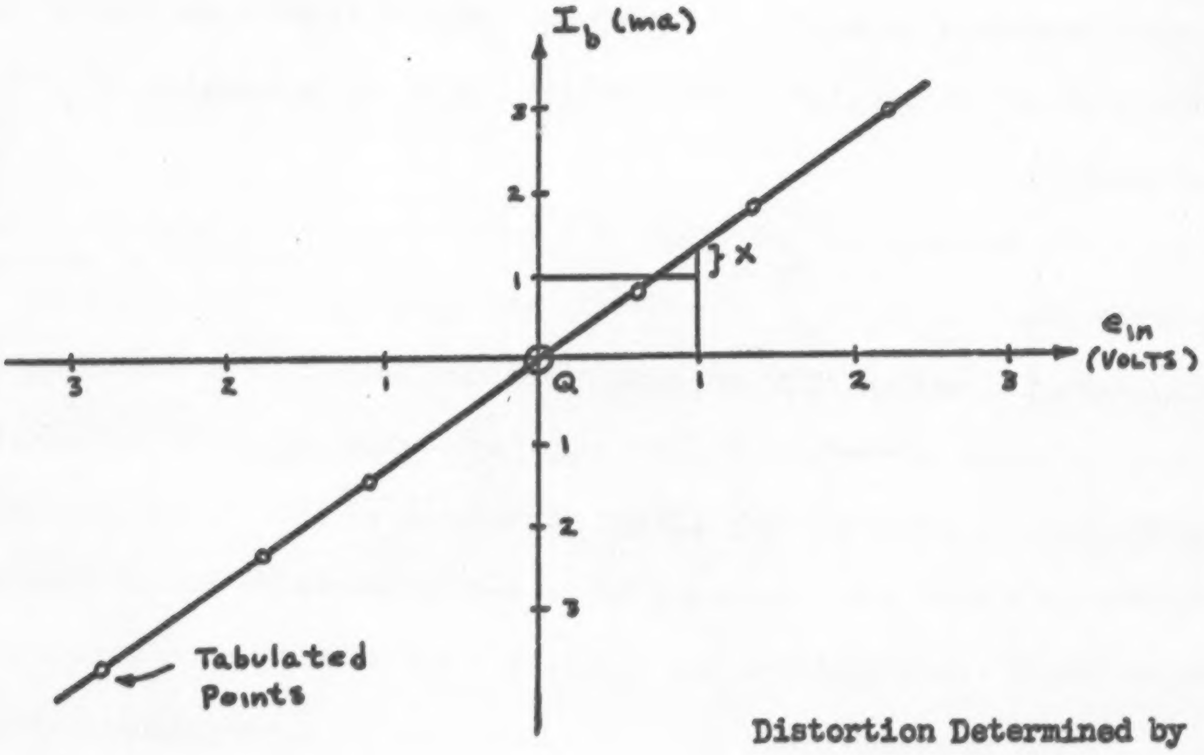
Fig. IV-4.

3) Still another method which was employed was to plot the plate current as a function of the input voltage for various combinations of R_L and R_k (decided upon by criteria other than distortion). Then the distortion was determined by noting the discrepancy between the peak values of the plate current response (measured about the Q-point as the zero or reference point) for equal amplitudes of driving voltage. This is illustrated in Fig. IV-5.

A variation of this technique was to plot the transfer curve:

$$v_{out} \text{ (or } v_b) = f(v_{in})$$

and then to determine distortion.



Distortion Determined by
the Discrepancy X.

Fig. IV-5.

4) There were other methods, mostly just solving simultaneous sets of network equations and tabulating data concerning the response parameters of the system $\left[E_b, I_b, E_c\right]$ for different circuits. These do not merit detailed description, being minor variants of methods already discussed.

The next phase of analysis was the evaluation of the parameter tolerances of the value for the adjustable potentiometer in series with R_k (R_k'). In handling tolerances and the value of R_k', the techniques employed by the engineers were almost identical to those of the students. One popular method was logarithmic differentiation. (See section III, page 6, paragraphs 3.) . Other methods such as single parameter variation, and the worst-case method of analysis (Section III, page 6, paragraphs 4, 5). The

The only difference between consultants' and students' analyses was that the consultants were perhaps more thorough, using a greater variety of network equations and making their results more formal by tabulating results more extensively.

In determining the value of R_k', there was again great similarity between the techniques of consultants and students. For consultant engineers the method of worst-case variation needed in R_k according to variation in other parameters (to set $v_{out} = 0$ when $v_{in} = 0$) was almost universal. There were very slight variations on this technique. Again the consultants were more thorough, using a more extensive set of analytical expressions and tabulating and plotting their results more than the students.

The last and final phase of the analysis, determination of the power ratings for the resistors, showed some discrepancy from consultant to consultant. Some calculated ratings based on Q-point values of current and voltage, while others calculated power ratings assuming the system was near cut-off (i.e. $I_b = 0$) or near saturation (i.e. $E_c = 0$). Still other consultants based calculations on R.M.S. values of current and voltage or peak values. Some of the engineers based their calculations on the assumption that the resistors were at their nominal value, while others considered worst-case values.

This concludes the analysis of the consultants' analytical solutions.

B. JOBSHOP Analysis

The amount of data concerning the consultants' use of JOBSHOP in their analysis is very small. For most of them the program was a new experience and they did not perform very elaborate analyses using the program. Their use of JOBSHOP was confined mainly to checking D.C. quiescent values of voltages and currents, and to making production runs of final designs. Use of the augmentation card to test the effect of variation in circuit parameters was almost non-existent and those who did try these techniques usually found their results disastrous because of their lack of ability to program properly. Because of the lack of data, this is all that can be said concerning this subject.

V. Comparisons and Conclusions:

As stated in Section I the purpose of this report is to compare the approaches of the students and the consultants to the direct coupled amplifier problem.

By reading Sections III and IV one can observe the similarities and differences in the approaches for specific phases of analysis. Now we would like to comment on some general over-all impressions of the data for this design problem.

Concerning methods of formal analysis one can readily see the similar and different techniques used by the students and consultants by reading Sections III and IV. The method of swinging several trial load lines around the point where all load lines crossed were common to both consultants and students. Also the criterion used for the selection of a final Q-point was very similar for both groups. The use of logarithmic differentiation in the error analysis phase of analysis was another technique used both by consultants and students. There was also a great similarity between the equivalent circuits used by the consultants and those used by the students. As mentioned in Section IV the main deviation of the approach of the consultants from that of the students was the more extensive and sophisticated use of graphical techniques and analytical techniques in analysis. Also, the greatest deviation of the students' approach from the consultants' approach was the more extensive and sophisticated use of JOBSHOP by the former in their analysis.

Looking at the consultants as a whole and students as a whole several general remarks can be made. As expected, because of their more extensive educational background and practical experience, the consultants were much more thorough and sophisticated in their analysis. They also tended to show more variety in their analysis than did the students. The consultants used a wider variety of analytical and graphical techniques in their analysis. The consultants also showed a greater tendency to put their results in a tabulated form than did the students. Also, there were a greater variety of techniques in some phases of analysis from consultant to consultant. There were very few instances where the basic approach of the students differed from student to student.

With reference to the JOBSHOP analysis of the problem, almost the reverse situation prevailed. Referring to the parts on JOBSHOP analysis in Sections II and III we see that the analysis of the students using JOBSHOP was much more complicated when compared to the JOBSHOP analyses carried out by the consultants. It should be noted also that by using JOBSHOP for determination of resistance values and tolerances, students in some ways compensated for their inability to carry out some of the sophisticated analytical and graphical methods of the consultants.

The findings as far as this problem is concerned can be summarized by saying that the consultant engineers showed a greater degree of thoroughness and finesse in solving the problem, but the students, using JOBSHOP and the limited experience, were almost as successful (in some cases just as successful) in solving the problem.

II.B.2 DESIGN PROBLEMS IN SUMMER SESSIONS.

STUDENTS VS. CONSULTANTS

2. PENTODE VIDEO-AMPLIFIER DESIGN

by WINTHROP SMITH

Purpose. The purpose of this report will be to study similarities and differences in the approaches of the students and experienced consultant engineers in solving a pentode problem. The same outline will be followed as for Problem 23.

Problem. A video amplifier having an overall voltage gain of 100 decibels is required for use in a television system. The overall amplification should be flat to within ± 3 decibels over the band extending up to 4 Megacycles per second.

For uniformity, it is decided to use 6SJ7 tubes throughout, with the grid-to-plate transconductance $g_m = 2$ mhos, the screen-to-plate transconductance $g_s = 0.1$ mhos, and the screen-to-plate current ratio $= 0.25$. The plate conductance g_p may be neglected.

The equivalent grid capacitance $C_g = 8\ \mu fd$ and the plate capacitance $C_p = 7\ \mu fd$. The plate-to-grid capacitance is negligible.

1). How many stages of amplification will be required for a Butterworth response?

2). Discuss possible alternatives using resistance feedback, shunt-peaking and series-peaking circuits.

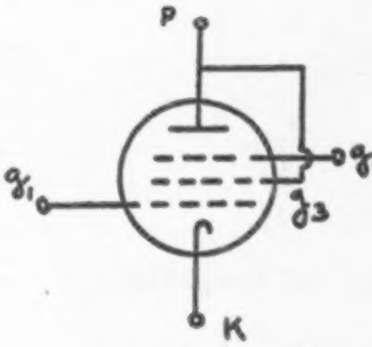
3). Design the high-frequency aspects of the amplifier using only resistance feedback to achieve the desired overall response.

Students' Approach.

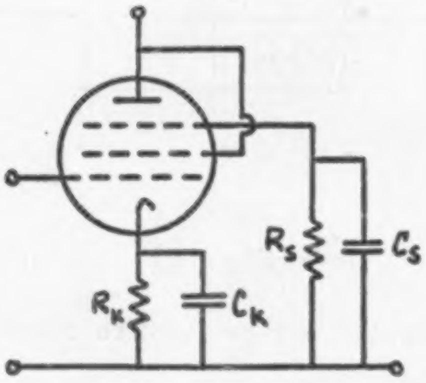
Overview of the Analysis and Design. The 6SJ7 pentode is a tube that has the customary five electrodes: the plate (p) or electron receiver, the cathode (k) or electron emitter, and the three grids that control the flow of electrons in the tube (Fig. 1). Notice that the No. 3 grid is kept at the same potential as the plate. First it was noticed that only the high frequency operation was specified in the design criteria.

Figure 2 shows the general tube arrangement for A.C. operation in an amplifying system. At high frequencies the capacitors used will be essentially short circuits so that the A.C. operating circuit looks like that in Figure 3. The linear equations that describe how this pentode operates can be written in a simple matrix formulation that pictures the pentode as a three-terminal "black box" (Fig. 4). With an elementary knowledge of matrix algebra, this matrix can be broken down into an arrangement of three 2x2 matrices which describe the pentode as an arrangement of three "triode type" devices (Fig. 5). This approach will be useful later when the pentode is programmed into JOBSHOP.

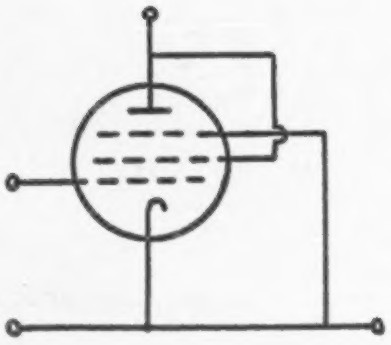
This equivalent circuit was examined by the students and it was noted that, with the cathode and grid No. 2 grounded, the system reduced to a triode that was peculiar because it had pentode gain characteristics and a very small plate conductance (Fig. 6). Thus, for high-frequency analysis, the pentode was considered as this peculiar triode.



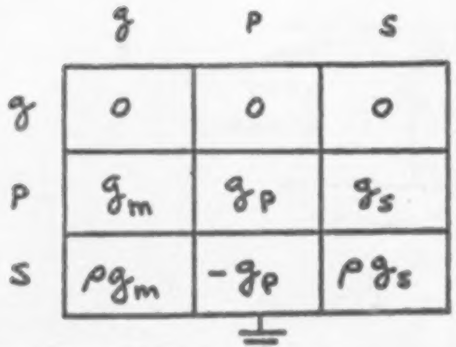
(Fig. 1)



(Fig. 2)

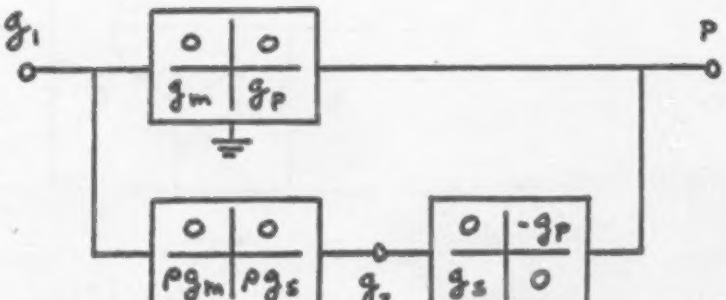


(Fig. 3)

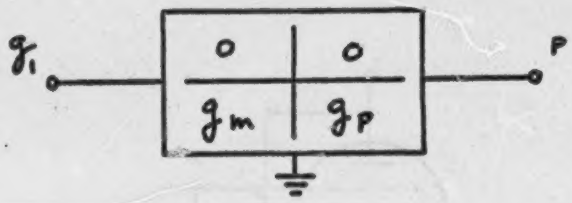


	g	P	S
g	0	0	0
P	g_m	g_P	g_s
S	ρg_m	$-g_P$	ρg_s

(Fig. 4)

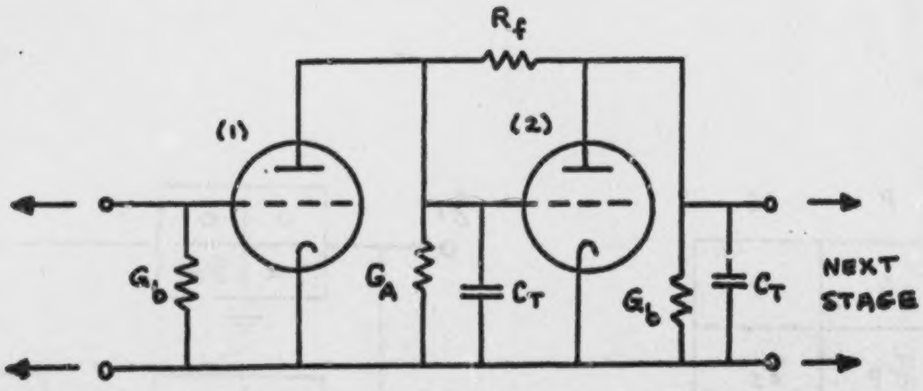

g_1
P
g_2
$\begin{array}{c|c} 0 & 0 \\ \hline g_m & g_P \end{array}$
$\begin{array}{c|c} 0 & 0 \\ \hline \rho g_m & \rho g_s \end{array}$
$\begin{array}{c|c} 0 & -g_P \\ \hline g_s & 0 \end{array}$

(Fig. 5)



(Fig. 6)

Since the problem specified resistive feedback, RC coupling circuits, and 6SJ7 tubes that have interelectrode capacitances of C_{pk} = 7pf. and C_{gk} = 8pf, the circuit that was used for the high frequency design looked like Figure 7.



(Fig. 7)

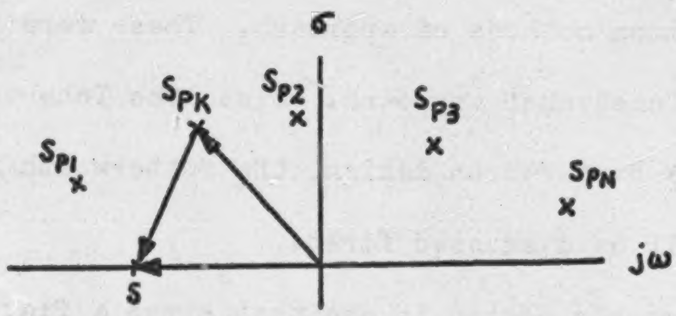
Tubes (1) and (2) represent a feedback pair and the grid resistor G_b was picked as 1 megohm only because this is a standard value used in this function.

The next step taken by the students was to decide on an approach to the design that would satisfy the desired specifications for the amplifier. There were two common methods of approach. These were the Butterworth approach and the Tchebychef approach. Since the Tchebychef design is developed from the Butterworth design, the Butterworth approach was followed first and thus will be discussed first.

The Butterworth design is one that gives a flat voltage gain characteristic in the pass band, and rolls off by 3 decibels at the bandwidth specification of the system. Since the gain variation within the band was specified as 3 db., this approach is very easily adapted to the problem. If the linear equivalent circuit of the tube is substituted for the tube, and the voltage gain of the system is solved for, a quotient of polynomials that are functions of frequency will be attained (viz).

$$\frac{e_{out}}{e_{in}} = A_{21} = \frac{N(s)}{D(s)}$$

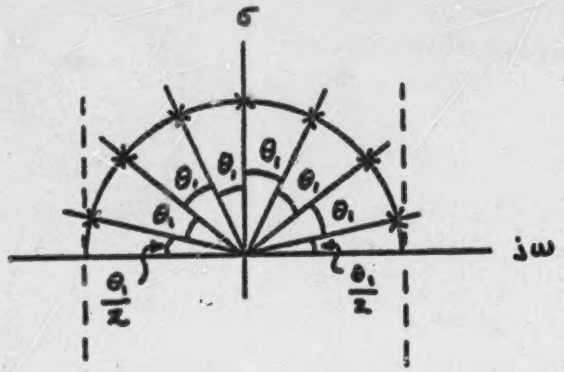
The poles of this gain function are the roots of the polynomial in the denominator. Since the poles of the system set the denominator of the gain function to zero, they control the response of the system to applied signals. (s is the complex frequency of the signal.) If the poles of A_{21} are plotted in the s-plane (Fig. 8), the value of the gain function can be determined because $D(s) = (s - s_{p1})\ (s - s_{p2})\ \ldots\ (s - s_{pn})$ where s_{pn} is a root of D(s).



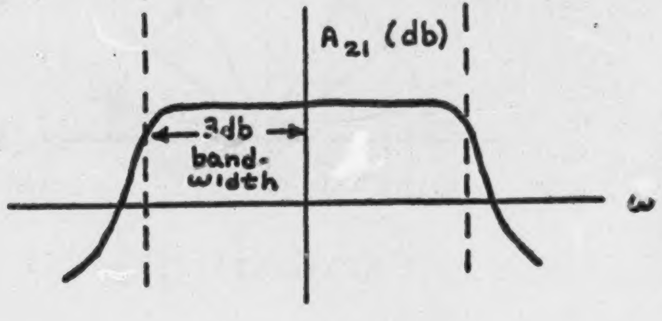
(Fig. 8)

Notice that if any frequency is picked on the s-plot, the vector between a pole and that frequency is $(s - s_{pk})$ so that these vectors determine A_{21} very easily.

Notice that in this circuit the N(s) in the numerator will not be a function of s since the circuit would have a gain of zero only at $s = \infty$ which is determined by D(s). If these poles are arranged equiangularly around a semicircle (Fig. 9), it can be shown that the gain function remains constant in the passband but drops off by 3 db. at the radius of the circle (Fig. 10). Thus, by making the radius of the circle equal to the desired bandwidth, the Butterworth design is obtained. By picking the circuit components so as to arrange the poles around the circle, a flat A_{21} characteristic is obtained. It turns out that the σ component of the pole is related to the interstage coupling and the jω value is related to the feedback resistors.


σ
θ_1
θ_1
θ_1
θ_1
θ_1
θ_1
jω
$\frac{\theta_1}{2}$
$\frac{\theta_1}{2}$

(Fig. 9)

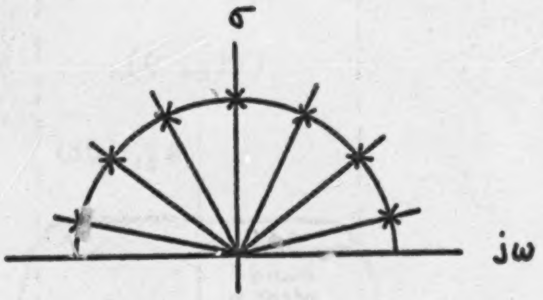

A_{21} (db)
3db bandwidth
ω

(Fig. 10)

The first step taken by the students was to find the number of stages necessary for the network. This was done by first computing the gain bandwidth product of a single stage similar to tube 1 of Figure 7.

$$\text{Gain bandwidth product} = g_m/C_T = (\text{gain/stage})(\text{bandwidth})$$

With this and the overall bandwidth of the amplifier, the gain per stage was calculated and translated to decibels. Knowing this and the overall gain needed, one can decide that seven stages are needed to fulfill the design. Thus seven poles, one pertaining to each tube amplifying section, were needed and were distributed on the semicircle in the proper manner (Fig. 11).



(Fig. 11)

As was mentioned above, the σ component was related to the total interstage conductance and the $j\omega$ component was related to the feedback resistor. Thus the necessary component values were then calculated for each stage. Since the feedback resistor was part of the total interstage conductance connected to the plate of each tube, its value had to be subtracted from the total before G_a, G_b were determined properly (see Fig. 7). Because these formulas were given in class rather than developed by the student himself, about one-third of the students neglected to perform this subtraction. This was of little consequence in most of the stages because G_a, G_b were so much larger than G_f. In one feedback pair, however, the values are very similar, and large differences in the interstage resistance occurred. When the value of G_f was subtracted, the values of G_f and G_a were so close together that a great deal of difference also occurred in the interstage components that were used. The component values attained for the other stages were very consistent except for the odd stage. Because

Student	$R_{1A}=R_{2A}$ Kilohms	R_{AF} Kilohms	$R_{1B}=R_{2B}$ Kilohms	R_{Bf} Kilohms	$R_{1C}=R_{2C}$ Kilohms	R_{Cf} Kilohms	R_4 Kilohms	SNORM	A_{21} (MAX.)	3db. Rolloff Frequency
1	11.8	14.9	4.25	23.2	2.94	74.7	2.65	1 Mc.	53.0 db.	2.77 Mcps.
2	34.5	18.15	4.47	14.2	3.07	74.7	2.65	1 Mc.	99. db.	
3	11.9	16.9	4.23	27.6	2.94		5.65	1 Kc.	110 db.	3.5 Mcps.
4	43.5	15.0	5.24	22.7	3.07	71.4	2.65	1 Mc.	101 db.	4.0 Mcps.
5	73.0	14.3	5.26	22.6	3.08	75.2	5.71	1 Mc.	108 db.	3.55 Mcps.
6	12.6	14.9	3.83	25.9	3.07	74.6	2.66	1 Kc.	98.9 db.	4.2 Mcps.
7	11.8	14.8	4.20	22.7	2.94	74.6	2.66	1 Mc.	52.6 db.	2.66 Mcps.
8	72.9	14.3	5.23	22.4	3.07	74.0	2.65	1 Mc.	101 db.	4. Mcps.
9	54.0	14.0	5.95	22.2	3.06	72.0	2.65	1 Mc.	101 db.	3.98 Mcps.
10	67.0	14.54	5.025	28.5	3.08	72.8	2.65	1 Kc.	102 db.	4. Mcps.
								1 Mc.	23 db.	3.16 Mcps.
								1 Mc.	23 db.	3.16 Mcps.
								12 Mc.	1 db.	1.5 Mcps.

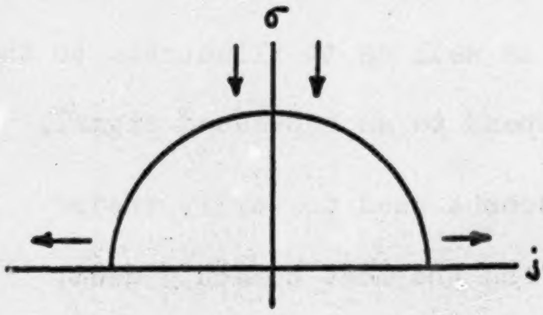
Table 1. Component values used by students and JOBSHOP values.

the odd stage was generally used as the output stage, the output capacitance varied from C_{pk} to C_t depending on the student. The above results can be seen easily in Table 1 above that summarizes the component values used by the students as well as JOBSHOP data that will be discussed later.

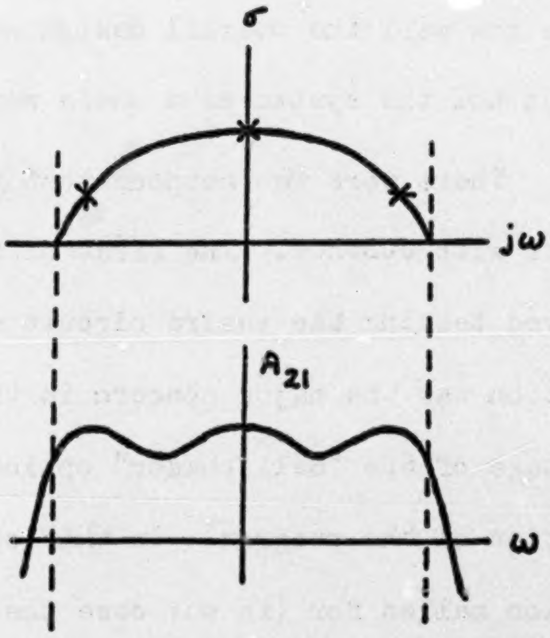
Notice that in the s-plane plot, the feedback resistors connect the plates of the stages whose poles are complex conjugates. Notice also that the troublesome poles (where G_a and G_f are nearly equal) are the ones closest to the $j\omega$ axis.

It was noted earlier that the problem area was also approached via a Tchebychef design. In this design the gain function has ripples in it that are controlled by the maximum peak-to-peak ripple allowable in the gain. To obtain this configuration, the poles of the system are placed on an ellipse. The ellipse used is developed from the Butterworth circle. The shrinking and stretching factors for the ellipse are calculated from formulas given in class. These formulas are dependent on the maximum ripple that is allowed. These factors shrink the σ values and expand the $j\omega$ values thus producing the proper ellipse for the ripple design. Notice that in this case the poles are all closer to the axis so the system gain will be increased. It is actually increased enough so that only six stages are needed for the design. Both of these Tchebychef designs were used by students. After the new pole values were found, the same procedure to establish the amplifier components (Fig. 12, 13) was followed as in the Butterworth design. The peak ripples in the gain function occur at frequencies where poles are located and half-way between these positions (maxima and minima respectively). This should be obvious since the circular arrangement produced a flat response and now the poles are closer to the $j\omega$ axis.

This concludes the discussion of the two approaches that the student followed in developing the video amplifier design. The table entered above shows the consistency in the components calculated and also exhibits the design verification by the computer that will be discussed next. It should be understood that the numbers in the table are shown to give a general trend in the student's results and nothing more.



(Fig. 12)



(Fig. 13)

JOBSHOP Analysis. The JOBSHOP program was used as a testing device by the students in this problem rather than a designing tool. This is most likely due to the specifications of the problem that was being solved. Because of these rigid specifications, the students decided to keep their components within the rigid specification of zero tolerance. Thus no effort was made to use JOBSHOP to decide how variations in the component values effected the required output specifications. Because of this and the rather simple calculations necessary to obtain the system components, the computer program afforded no real value to the student as far as developing his initial design. However, because of the awkwardness of dealing with the system equations as a whole, the program was used extensively as a test to see how well the overall design worked, as well as to illustrate to the student how the system as a whole would respond to an impressed signal.

There were two methods that the students used to verify their results with JOBSHOP. The first of these, and the most commonly used, involved testing the entire circuit with the program. The high frequency operation was the major concern in this design, so the students took advantage of the "call phasor" option. This is the frequency testing operation of the program. In this operation the computer takes the function called for (in our case the voltage gain function, A_{21}), substitutes values for frequency, and plots the resulting points as a function of frequency. Because the function will have real and imaginary parts it would inherently involve a three-dimensional plot. So, the computer plots the amplitude and the phase separately as functions of frequency. The computer program performs this operation on such variables as input and output impedance, and voltage and current gain. It also has the advantage that the amplitude as well as the frequency can be plotted linearly or logarithmically. Because the voltage gain was the only function of importance to the student in meeting the given specifications, it was the only function that was utilized as a system tester.

Because the pentode as such cannot be realized on JOBSHOP, it is first reduced to an arrangement of three triodes (see Fig. 5) and is submitted in this manner. Since the system is operating at high frequencies, this arrangement reduced to one triode that had a pentode gain (see Fig. 6).

With the pentode implemented as the triode, the program develops a set of independent equations that describe the system. Because of the large values of frequency at which the system may operate, the equations may become very large and cumbersome to handle. This difficulty is removed by normalizing the frequency of operation. The operator specifies an SNORM value in the neighborhood of operation of the system and the computer multiplies both the numerator and denominator by the appropriate factor of SNORM. By this we mean that the s^n factor is multiplied and divided by $(SNORM)^n$, and so forth. Then the normalized frequency of the equation becomes $(s/SNORM)^n = (s_1)^n$. This is the operation that can cause problems in the functioning of the JOBSHOP program. While it normalized the s variable, it also introduced a constant multiplier of $(SNORM)^n$ into the $(s_1)^n$ term of the system equations. Thus, if the value of SNORM is set at 1000, the problem of large numbers in the equations again occurs. Since the higher order terms will predominate, when the equation is stored in the computer, the lower order terms may be lost. This is the so-called "round off" error that occurs.

The scaling of SNORM in the program is completely dependent on the scaling of the resistance and capacitance components. So, to avoid the problems mentioned above, most of the students rescaled their components units so that SNORM = 1. Since 1/RC has the units of cycles per second (i.e. frequency), if the resistance unit were kilohms and the capacitance units were microfarads, then SNORM = 1 would mean that SNORM was one kilocycle. In reference to the chart displayed above, notice that students 1, 7, and 10 had a problem in attaining the proper gain even though the components they used correlated with those of successful students. In each case the problem was that of SNORM being set equal to a value greater than one. It was set equal to at least one thousand in each case. Thus round-off destroyed the proper functioning of the amplifier. In each of the other cases, except student 8, SNORM was set to one.

Student 8 avoided the round-off problem in a different manner. He approached the problem in the alternate manner mentioned. This involved splitting the system into two parts, running them separately and then manually combining the results of each half. This approach was followed mostly by the students who used the Tchebychef design, because this design (as mentioned) could be attained with an even number of six stages. Student 8 used the Butterworth design and split his system up with two feedback pairs in one half and a feedback pair and the odd stage in the other half. He set SNORM = 1000, but, because the equations for each half now did not involve terms of such high order, the round-off problem never occurred in a manner that was detrimental to his results. This can be seen by comparing his results to those of similar designs in the display chart.

Thus the students used the frequency response operations of the computer to check the validity of design. Because the voltage gain response supplied him with not only the gain function but its bandwidth, it was sufficient to check the design with the specifications. Since the student knew that the roll-off was in the neighborhood of four megacycles, the plots usually ran from 100 kilocycles to 10 megacycles so that the midband gain could also be determined. Because the frequency was plotted logarithmically, it was difficult to accurately determine the 3 db. roll-off frequency. Therefore most of the students ran a frequency response in the neighborhood of the roll-off once that region had been more accurately established.

As can be seen from the discussion above, the video amplifier presents the student with a challenging engineering problem. It is a problem that requires the student to plan an attack based on the specifications that he must meet. Obviously this involves a knowledge of methods of attacking the problem as well as a confidence that the design he develops will function in the desired manner.

The primary objectives of the design course were to present the student with methods of analyzing the performance of a circuit as well as give him a feeling for using these methods in designing a circuit to perform an engineering task. Therefore, JOBSHOP plays an important role because it develops the student's feeling for how the physical circuit functions. Often this feeling can be lost in mathematical manipulations and this loss decreases the engineering value of the designer. This is particularly true in a circuit like the video amplifier because it contains a large amount of circuitry.

The voltage gain function of the amplifier involves the quotient of two polynomials in s, each containing a large number of unknown inter-stage and feedback components. Because the student was aware of the Butterworth and Tchebychef approaches to design, and was able to verify his design on JOBSHOP, the problem of designing the amplifier became an engineering problem. This is opposed to a tedious analytical puzzle that results from solving the problem from a purely mathematical standpoint. The ability to easily verify design results gives the designer a feeling of confidence that is necessary in the development of a competent engineer. Thus the JOBSHOP student has gained an advantage over students at a similar academic level because he is familiar with the above design techniques and has gained a competence in using these techniques through the use of the JOBSHOP program.

Consultants' Approach. The consultants' approach to the design of the video amplifier was generally in terms of the physical device rather than the four-terminal black box.

The first thing decided on was the number of stages necessary to satisfy the bandwidth and gain specifications. In order to satisfy the specification that the gain be flat to within 3 decibels over the specified bandwidth, the Butterworth design was chosen. Because seven stages were needed, it was decided that three resistance feedback pairs would give the necessary conjugate pairs of poles to satisfy the Butterworth pole distribution.

Two different methods were used in calculating the interstage component values that would fit the pole positions. Actually, the second approach proved unsuccessful and the consultant using this approach reverted back to the first method. The first method involves developing the node equations for the feedback pairs and fitting the unknowns in these equations to the pole positions. This method proved very successful and gave values very close to those in Table 1. The second method involved using equations for feedback pairs developed in a paper written by Dr. Huggins (The Natural Behavior of Broadband Circuits, ERL Report E5013A, 1948). This method turned out to have a number of pitfalls. The primary difficulty was the inability of the consultant to properly interpret the parameters of the equation. This produced false values for the interstage components thus producing a gain function that was unsatisfactory. Secondly, the equation itself had an error in it that was discovered after the consultant (using this approach) reverted back to the first method of attack. In each case the error was detected from the JOBSHOP program output.

JOBSHOP as used by Consultants. The JOBSHOP program was used by the consultants as a tool to check the circuit designs that they had developed. They used the phasor plot of the voltage gain function to discover if their design had met the gain and bandwidth specifications.

One consultant developed the roundoff problem discussed in the students' report but it occurred for a different reason. In the high-frequency equivalent circuit the consultant included the seven cathode circuits rather than assuming that they acted as short circuits. This meant the inclusion of seven 50 microfarad capacitors in the circuit causing the gain function polynomial to be of the order of $(s_1)^{14}$ rather than

$(s_1)^7$. Since the larger s terms can completely dominate the function and can cause the same roundoff that was suggested in the students' report, the consultant obtained results that were completely erroneous. Because of this, he calculated the gain and plotted it graphically. He found it to be correct and postulated that the problem was in the method of system analysis. It was interesting to notice that when the consultant calculated the mid-band gain by hand he neglected the cathode circuitry. Thus had he tried to analyze the system on the computer in the same manner he used in the hand calculation he would have received results confirming his design procedure.

The JOBSHOP program also proved useful to the consultant who had problems with the equations obtained from Dr. Huggins' article concerning interstage components. Each time he completed a design it was run on the computer and it was found that the gain and bandwidth did not fulfill specifications. Thus the consultant quickly obtained an inkling that his design was in error. He followed this procedure until he decided that the borrowed equations, rather than his design, were in error.

He then reverted to developing the equations himself and proceeded to successfully use JOBSHOP to verify his design.

The JOBSHOP program was definitely an asset to the consultants in their development of the design of the video amplifier. Not only did it provide an error check on their design calculations but it provided a check on the equations they used in designing the amplifier. Thus not only is JOBSHOP a valuable tool in teaching design, but it seems to be an asset in actual design work.

Comparison of the Students and the Consultants. In general the students and the consultants attacked the problem in the same way. Both groups began by determining the number of stages needed and then the gain per stage. Then the choice of design type was made. The students were somewhat divided between the Butterworth (about 75%) and the Tchebychef (about 25%) designs while the consultants chose the Butterworth design in each case. Both groups then proceeded to use the -plane plot (see Fig.11) to determine the interstage components. The problem was then introduced to JOBSHOP to check the accuracy of the design procedures.

While the methods of attack were nearly the same, the tools used were very different. The consultants relied heavily on the node equations of the pentode stages while the students used formulas developed in class and based on the four-terminal blackbox representation of the vacuum tube discussed in the students' report (see Figs. 4, 5, 6). Both students and consultants developed the roundoff problem in JOBSHOP because they were unfamiliar with the computer processes used in the operation of the program. In order that the program be used effectively and efficiently it is necessary that the processes that JOBSHOP performs be understood by the designer.

The other aspect of this problem that showed a similarity between the students and the consultants was their use of the design equations. At one point in the design development the students used a design equation but used it incorrectly because they interpreted the terms of the equation improperly. At another point in the design the consultants used a design equation incorrectly for the same reason. This points out an interesting characteristic of the students that seem to linger with the post graduate engineer. That is his willingness to use equations that he is unfamiliar with in order to alleviate tedious calculations.

Conclusions. The JOBSHOP program is obviously a tool that can be used advantageously in teaching design as well as in developing designs.While it alleviates many of the problems in design work it introduces one that must be conquered to use the JOBSHOP program effectively. That is the problem of understanding the operation of the program as well as its limitations. The complete documentation (with worked-out examples) now provided in Sections I.B and I.C should meet this need.

II. B.3 THE QUESTIONNAIRE GIVEN TO SUMMER SESSION PARTICIPANTS

NOTE: The following questionnaire was given, with enough space following each question for the student to write a lengthy response.

" Directions. The purpose of this summer experiment has been to see whether principles of electronic design can be taught to undergraduate students in a short time by a combination of lectures and JOBSHOP. Lectures have described basic theories and given examples. JOBSHOP has been made available as a tool to assist students in acquiring the skills of design through experience.

We would like to discover how much assistance JOBSHOP has actually been in leading you toward becoming a competent designer. We are very interested to learn your reaction to the JOBSHOP design sessions and also to the JOBSHOP simulation program.

To help you in organizing your thoughts concerning the value of JOBSHOP to you, we have compiled a list of questions. It will be necessary for you to think back independently over the designs you have completed in the last few weeks in order for you to answer the questions in sufficient detail. Only careful and detailed answers will be of value to us.

Please consider each question carefully before answering it. Also try to give us any concrete information you can think of pertaining to your JOBSHOP experience, even if there is no question about it below. Devote sufficient time and thought to your answers, and do not answer merely "yes or no". Part of your responsibility as a subject in this experiment is to report to us in detail the ways in which you have used JOBSHOP and the ways in which JOBSHOP has been useful to you in learning to design.

Questions

1. Have you worked by yourself or with others? If with others, who and to what extent?

2. Have you tried any other problems beyond those assigned, either in June-July 1964 or earlier in I.S. and D.?

3. If you yourself were teaching a course in circuit design, would you use the JOBSHOP simulation (Yes or No and why. Please be very explicit.)

4. a. Have you been able generally to go back over your lecture notes, and understand what has been presented to you?

   b. Do you feel that you have a complete set of lecture notes?

   c. How many lectures have you missed?

   d. What outside influences have kept you from putting in as much time on your designing as you would have liked to?

5. What did you like the most about the JOBSHOP sessions? What did you like the least?

6. Think back over your experience of the summer and abstract the general step-by-step approach that you feel you have used in answering the problems we have assigned to you. Concentrate on the part which JOBSHOP has played in this approach. Try to give as much detail as possible. You may find it helpful to think of a specific design problem and describe your strategy of solving it.

7. What difficulties have you encountered in the mechanics of coding a problem to be run on JOBSHOP?

8. What procedures have you devised from time to time that you feel JOBSHOP was unable to carry out?

9. What difficulties have you found in evaluating the results returned to you by JOBSHOP?
10. On the average how many runs with JOBSHOP did you need before you felt that you had obtained an adequate design?
11. How did you decide when your design was completed adequately?
12. Do you feel that, in order to acquire skill as a designer, it is essential to have a more experienced person around who can answer your questions? Or do you feel that, with the aid of JOBSHOP you managed to obtain adequate results alone or by consulting other students?
13. To what extent do you feel that JOBSHOP would be useful in solving problems arising in your hobbies or in other courses?
14. Do you feel that JOBSHOP has assisted you in understanding the operation of electronic circuits above and beyond the understanding you have acquired in lecture?
15. Have you discovered any principles valuable in designing that were not specifically mentioned in lecture? If yes, what are these? If no, why do you think this is so?
16. To what extent do you feel, not being concerned with the actual procedures involved, that you understand what JOBSHOP does in providing you with the results you request?
17. Do you think that knowledge of FORTRAN has helped you in using JOBSHOP? Do you think it would be a serious disadvantage not to know FORTRAN?
18. Do you feel that it was necessary for you to have a fairly thorough analytical design before you used JOBSHOP?

19. Records on the last page show how often you went on the computer in June. The class average for this period is 80. Compare your usage with that for the class and explain the significance of this.
20. To what extent do you feel that you have learned to design?
21. Do you feel that you could use JOBSHOP to design circuits using active elements other than the vacuum tube?
22. Do you think you could have advanced as far as you have without JOBSHOP, but with some other specific assistance?
23. Have you any suggestions for improvements and/or modifications to JOBSHOP which would make it a more valuable tool?
24. Is the JOBSHOP coding form satisfactory? Why not?
25. What is your reaction when JOBSHOP corroborates one of your designs?

Summary of Answers

After questionnaires were filled in, they were examined and returned to student for more complete or explicit answers where necessary. A summary of their replies is given in Table II. B.3.1

Some of the questions were very pertinent to the usefulness of the JOBSHOP program in teaching design. For instance, Question 3 "If you yourself were teaching a course in circuit design, would you use the JOBSHOP simulation." This was answered "Yes" by all students. A sample convenient to the question is: "Even if the theory were not clear initially, one could proceed with the general strategy presented by the worked problem. The insight gained by following the problem solution could clear up the hazy points of the theory".

Table II B.3.1

Questions

Student #	1	2	3	4A	4B	4C	4D	5	6
1	Mostly alone	yes	yes	yes	yes	none	part-time job	a chance to learn	6
2	others	yes	yes	yes	yes	none	p.m. class	2 liked 2 disliked	6
3	others	yes	yes	yes	yes	7	Yes-part-time job	2-yes 3-no	6
4	alone	yes	yes	yes	yes	none	p.m. school	2-yes	5
5	others	no	yes	yes	yes	none	part-time job	1-yes 1-no	3
6	alone	yes	yes	yes	yes	none	course at J.H.U.	3-yes 1-no	7
7	alone	no	yes	no-?	yes	none	night school	liked lectures	5
8	alone	yes	yes	yes	no	1	p.m. school	1-yes 1-no	1
9	alone	no	yes	yes	yes	2	Sociology course	1-yes 2-no	5
10	alone	no	yes	yes and no	yes	none	none	computer output	4
11	others	one	yes	no	no	none	none	1-yes 1-no	12+
12	mostly alone	no	yes	yes	yes	yes	none	none	7+
13	others	no	yes	yes and no	yes	2	sports	computers	4+
14	others	yes	yes	yes	yes	none	slow worker	JOBSHOP 1-no	3+
15	alone	no	yes	yes	yes	none	none	knowledge weather	4+
16	others	no	yes	75%	75%	2	none	working lectures	4
17	others	no	yes	yes	yes	none	no none	yes and no	6
18	others	no	yes	no	no	none	p.m. work	work as a team	10

Table II B.3.1 (continued)

Student #	1	2	3	4A	4B	4C	4D	5	6
19	others	no	yes	yes	yes	none	p.m. school	lectures	5
20	others	no	yes	yes	yes	none	none	to develop explore	5
21	mostly alone	little	yes	yes	yes	none	girls		7
22	mostly alone	no	yes	no	yes	4	none	working designs	

Table II B.3.1 (continued)

Student #	7	8	9	10	11	12	13
1	2	none	graphs	5-6	--	yes	yes
2	2	variables	errors-program	4-5		yes	yes
3	2	none	few	2-3		yes	yes
4	2	none	graphs	3-4		yes	yes
5	1	none	none	2-3		yes	none
6	1	component	lack of storage	4-5		no	EE lab
7	2	none	coding problem	4		yes	design project
8	1	none	curve output	1-2		yes	circuit problems
9	1	output voltage	graphs	3		no	yes
10	3	none	values of resistors	2-3		yes	lab work
11	1	none	log scales	3		yes	HiFi
12	none	none	none	1-4		yes	lab courses
13	value of snorm	none	log plots	1-5		yes	lab
14	none	1	graphs	1-2		yes	none
15	very few	output	none	10-12		yes	electronics
16	3	none	graphs	2-3		yes	labs
17	2	circuit source	reading graphs	1-10		yes	science and engineering
18	several	none	graphs	5-6		yes	none
19	4	parameter values	graphs	several		yes	no
20	voltage source	vacuum tube design	none	1-2		yes	yes
21	snorm	tube design	graphs	2-3		yes	yes
22	unistor	none	node equations	3		yes	tolerances on circuit parameters

Table II B.3.1 (continued)

Student #	14	15	16	17	18	19	20	21
1	yes	no	yes	no	yes	below	learned a lot	yes
2	yes	no	yes	no	no	above	basic elements	yes
3	no	yes	yes	yes	yes	below	quite amazed	yes
4	yes	no	yes	no	no	below	can now design	yes
5	yes	no	yes	no	yes	below	still need help	yes
6	yes	yes	yes	no	no	below	actual knowledge	yes
7	yes	no	somewhat	no	yes-no	above	could become good	yes
8	yes	no	vague	no	yes	above	solve similar problem	yes
9	no	no	limited sense	no	yes	above	experience	yes
10	no	no	?	no	yes	below	learned a lot	yes
11	no	no	fairly well	no	yes no	above	more understanding	yes
12	yes	no	yes	no	yes	below	gained knowledge	yes
13	no	no	vague	no	yes	above	learned a lot	yes
14	yes	no	yes	no	no	below	more study	yes
15	a little	no	fair idea	no	yes-no	below	advanced	yes
16	no	no	well enough	no	yes	above	no difficulty	yes
17	no	yes	yes	no	yes-no	above	confidence	yes
18	yes	yes	very well	no	yes	above	basic procedures	yes
19	yes	yes	yes	no	yes	above	should be able to design	yes

Table II B.3.1 (continued)

Student #	14	15	16	17	18	19	20	21
20	yes	yes	very little	no	no	below	average	yes
21	yes	yes	hazy idea	no	yes	above	helped greatly	yes
22	yes	yes	basic understanding	no	yes	below	systematic approach	yes

Table II B.3.1 (continued)

Student #	22	23	24	25
1	yes	yes	yes	happy
2	no	no	no	accomplishment
3	no	yes	no	satisfaction
4	no	no	no	satisfaction
5	no	no	yes	relief and surprise
6	yes	no	yes	jubilation
7	yes	no	no	pleasing
8	yes	no	yes	pleased
9	no	yes	yes	satisfaction
10	yes	yes	no	surprise and relief
11	yes	yes	no	accomplishment
12	no	none	yes	well, that's done
13	yes	yes	yes	always nice to see
14	no	no	yes	jubilation
15	yes	yes	yes	satisfaction
16	no	none	no	relief
17	no	yes	no	satisfaction
18	no	yes	no	satisfaction
19	no	yes	yes	quite pleased
20	no	no	yes	success
21	no	yes	yes	elation!
22	no	larger # of nodes	yes	satisfaction

Two students felt it necessary to go into the laboratory and construct actual physical devices on the first problem that was assigned. That is, they did not think that the simulation could possess for them the degree of conviction possessed by a working device. On the questionnaire, and in a subsequent interview, they stated that the lack of conviction was very temporary. They felt no need to go to the laboratory on later designs, and stated that they felt little was accomplished by this excursion for the first problem.

The work style of students varied as reported in the analysis of students' performances on the two comparison problems (Section II.B.2). Their perception of this was fairly veridical. To the question asking how many runs in JOBSHOP were required (Question 10), for the 22 students the average figure listed was close to 4. There is great variance, however, with some students requiring 1-2 runs, and one student reporting 10-12. One of the most competent students with this program replied "1-10", while another who achieved good designs replied "1-2". The number of runs needed may reflect work style. Careless coding can produce 3 or more runs that are useless for design purposes, and elaborate preliminary calculations may replace some initial runs.

The questions that relate most closely to our major research objectives are Questions 14 and 15.

> "14. Do you feel that JOBSHOP has assisted you in understanding the operation of electronic circuits above and beyond the understanding you have acquired in lecture?"
>
> "15. Have you discovered any principles valuable in designing that

> were not specifically mentioned in lecture? If yes, what are these?

The answers to Question 14, broken down by grades achieved in the Introductory Systems Course are:

Question 14

		Yes	No	
	A	5	5	10
Grades	B	3	2	5
	C	7	0	7
		15	7	

The poorer students are unanimous in stating that JOBSHOP increased their understanding. The "A" students split in half on this question. This association between grade-level and helpfulness of JOBSHOP is significant beyond the 5% level. Needless to say, a teaching aid that services the poorer students holds interest for practical educational work.

The answers to Question 15 are not so encouraging. About one-third of the students (8 out of 22) responded affirmatively.

Question 15

		Yes	No
	A	5	5
Grades	B	1	4
	C	2	5

It appears that the "B" and "C" students, although finding the program helpful for learning, did not feel that it aided them in discovering design principles. The "A" students are a rather peculiar group, because two of them who responded negatively to Question 14 responded affirmatively to Question 15 - they felt the program helped them discover design principles not mentioned in lecture but they did not feel the program aided their understanding of electronic circuits. It may be that these students of very high ability comprehend so rapidly and completely, that any redundancy in presentation is unnecessary. Yet given a tool, like JOBSHOP, they will be enabled to pursue a topic further than with conventional sources of information. It is pertinent to note here that senior students, not connected in any way with this project, have requested permission to use the JOBSHOP program. The main discouragements to more complex uses are two: (1) the program can handle linear devices only, and (2) there are no transients in the program because the space in the computer is entirely used up by the program as it now stands.

About two-thirds of the students (14) responded favorably to Question 22 - that JOBSHOP helped them more than some other form of assistance to advance to their present level of competence.

Discussion of Questionnaire Results. The general tenor of the answers is positive, and in the students' opinion the JOBSHOP program is for some a desirable, and for others a necessary teaching aid. There is undoubtedly some favorable bias as far as students' opinions are concerned, however, since they were a hand-picked group who volunteered to participate in the sessions.

Although it is impossible to provide a "control" group of the standard sort who were taught by more conventional methods and thus would make an objective comparison possible, we are of the opinion that JOBSHOP allowed the presentation of much more material in terms of absolute volume and also more complex material. In a matter of nine weeks, students who knew very little circuitry were brought to a point that they could solve successfully problems of sufficient complexity to challenge experienced designers.

The experience with the survey group has yielded information that improves the usability of the program.

SECTION III

Psychological Studies Related to JOBSHOP Research

INTRODUCTION

A number of psychological studies, tangential to the main topic (evaluation of JOBSHOP), were possible while this research was in progress, and the opportunity was taken to carry out such studies. They are reported separately in this section. For the most part they are unrelated to one another, so each is reported in a self-contained manner.

An attempt to carry out one experiment was unsuccessful, because the experimental maneuver turned out to be not feasible. The hypothesis at which the experiment was directed is important, however, and a brief account of it is therefore included here.

It is well-known that meaningful material is retained longer than nonsense material and also is more quickly learned in the first place. A number of explanations, differing in detail, have been advanced. Without reviewing these explanations at length, one can note that re-coding is a central concept in most of them. That is, meaningful material can be coded in chunks, probably larger units, than nonsense material because previously established habits support cohesion of the internal features of chunks. This re-coding also may make the chunks resistant to extinction because 1) the chunks can be made relatively independent of one another and 2) the chunks can readily be attached to other overlearned materials. They participate vicariously in the overlearning bonus stemming from the concepts to which they are tagged.

Electrical engineering material of the kind included under the topics related to electronic circuits appeared to offer a medium where we could study the benefits accruing to meaningful learning via re-coding.

Specifically, a signal can be acted upon by a filter which changes the original signal. Much of electronic design consists of inventing filters to accomplish specific purposes. The filters can be represented by mathematical statements, and manipulations of the mathematical statements corresponds to re-arranging or otherwise changing the circuits of the filter. One way to proceed in design is to build an actual circuit and then, more or less by trial and error, change components, change the placement of components, and so on, until a desired effect is achieved. This has obvious drawbacks.

Another approach is not to deal with the physical circuit itself but rather to describe its natural behavior. For most linear systems, this natural behavior is characterized by certain natural frequencies for which the system refuses to respond at all. These frequencies are described by complex numbers, the real part of the number indicating the growth rate of the oscillation, and the imaginary part the oscillation rate. Then it is possible to encode any of the system functions, which describe the various input-output relations of the system, into a very simple pole-zero diagram which vividly portrays as a geometrical picture how the system will behave. This pole-zero diagram is equivalent to the mathematical system function, and may be related directly to the parameters of the physical circuit. However, the pole-zero diagram encodes in purest possible form the response characteristic and suppresses all irrelevant detail.

The link between the pole-zero diagram and the circuit diagram is that from either, one may calculate the response of the circuit to a specified input signal. Superficially, there is no resemblance whatsoever. The circuit diagram shows an interconnected collection of resistors, vacuum tubes, capacitors, etc., whereas the pole-zero diagram is simply a plot of some points on the complex plane. The correspondence between these two representations is not at all obvious. Yet, most experienced engineers come to think of these two representations as different views of the same system - the one showing the relations between the things and the other, the relations between the signals arising in the circuit. It is intriguing to consider how a student coming to these considerations for the first time can handle such radically different representations.

Another approach is to manipulate the mathematical representation of the circuit to achieve desired effects. It happens that many signals can be decomposed into parts that combine additively. Each of these signal portions can be fed into a filter and the outgoing signal obtained by adding up the pieces of the original signal after they have passed through the filter. In design it is clear that this process might become extremely complicated, especially when many filters are attached to one another. However the mathematics will often produce expressions that have numerators and denominators of factors.

Just before students were to be introduced to the pole-zero formulation, but after they were relatively familiar with analysis of RLC circuits, we decided to try an experiment to see if we could measure the "conceptual benefits" of the pole-zero approach. The hypothesis was that a pole-zero approach would permit more efficient solution of circuit design problems than the more cumbersome approach via actual circuitry. The students were randomly divided in half to implement the following design:

Students:	Group A -	Pole-zero formulation first; circuitry formulation second.
	Group B -	Circuitry formulation first; Pole-zero formulation second.

Two problems thought to be of equivalent difficulty (actually the circuits were duals of one another) were used as the basis for the two successive formulations presented to groups A and B.

It turned out that the criterion test, given after the presentations, was useless. There was not enough variance in the test to permit any comparisons. The main drawback is apparently that these concepts require lengthy presentation and so other sources of variance tend to outweigh variance that can be interjected by the experimental maneuver.

SECTION III.A

DOMINANT WORD ASSOCIATIONS ACCORDING TO GROUP MEMBERSHIP

Word association data have lately served to buttress theorizing about language acquisition, verbal learning and concept formation, and even about human information storage and retrieval. Johnson's (1964) recent demonstration of a strong bridge between structured word associations and problem solving capability is a provocative experiment, and one directly related to earlier demonstrations that response dominance correlates positively with efficiency of concept utilization (Romanow, 1958; Underwood and Richardson, 1956). This paper reports a comparison of word association responses to ambiguous stimuli, showing that specialized and technical knowledge of two very different content areas yields a constriction of associations.

Design and Material: Two comparable groups of Ss were made up of college freshmen and sophomores. Group A had recently completed a course in introductory social psychology, while Group B had recently completed an engineering course in introductory systems with emphasis on electrical circuits. Group A students were enrolled at Goucher College, and Group B students at Johns Hopkins University.

Certain key words for each group express salient concepts covered in the respective courses, but at the same time these words are familiar to all college students in more general contexts. "Achievement" is a particularly relevant word for social psychology students (e.g. "achievement motivation", "n Achievement") but also the word is well known to students not enrolled in psychology courses. (See Class I stimuli, Table 1.) Similarly, "plate" is a very familiar word apart from its meaning as a part of a vacuum tube. (See class II words.)

These ambiguous words, with both common and technical meanings, offer a means of discovering response dominance in each group brought about by training. By administering all words (Class I and Class II) to both groups, one can establish the amount of response dominance in non-trained but comparable individuals. That is, "plate", "current", etc., when administered to social psychology students will produce patterns representative of non-engineering students, and "achievement", "role", etc., when administered to engineering students will accomplish the same end for non-psychology students.

Group A and B consisted exclusively of females and males, respectively, and therefore a third set of stimuli (see Table 1, Class III) was included as a control on female-male differences. These stimuli were words judged technically relevant for both electronic circuitry and social psychology. "Power" and "bias" are two examples of words of this kind. The primary response for each group bears out the validity of judgment concerning Class III words. "Power" elicits "watts" from the engineering group, and "authority" from the psychology group. There are well-known sex differences in word associations, and these doubly-relevant words (Class III) therefore provide a control for sex differences.

Method: Groups A and B each consisted of 24 students. They were given sheets containing stimulus words alternating from Class I to Class II, insofar as possible. (Verbatim instructions resemble closely those reported in Entwisle and Forsyth (1963)).

Results: Responses were tabulated and are summarized in Table 1. The number of different responses and the most frequent response for the three classes of stimuli are given.

There is a noticeable constriction of response, or response dominance, in each group for words relevant to major concepts of the training materials. For Class I words, 11 out of 12 stimuli yield fewer different responses for the social psychology students. The one exception is "snow". This result is significant beyond the .01 level using a sign test.

Responses are constricted in the opposite direction for Class II words, relevant to electronics. In 10 out of 12 instances, fewer different responses are given by the engineering students, and this difference is statistically significant beyond the .01 level also.

For words relevant to both groups, Class III, there is about equal response dominance. This makes it very unlikely that the sex of the respondent rather than prior training is responsible for the differential response dominance.

Discussion: Response dominance increasing with training, and presumably the change in primary response with training, need to be explored in relation to practical educational problems. Methods for producing response dominance need investigation in the light of Johnson's finding that problem-solving ability is related to associative patterns. The best teaching method for inculcating definitions may not be the same as the best method for teaching concept manipulation.

The findings reported here may offer a methodological suggestion. In some experiments it might be advantageous to replace "examinations" with word association tasks as a criterion measure in training experiments. Often a test or other examination-like procedure is contained in an experiment to measure outcomes of two different training procedures, but for some groups of Ss (notably college students) tests have undesirable anxiety-producing properties. A cognitive measure that is less structured may offer more precision, although of course the validation task is a serious drawback.

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Table 1.

The Number of Different Responses and the Most Frequent Response to Three Classes of Stimulus Words

Word	T-L* count	No. of different responses		Most frequent response	
		F	M	F	M
Class I -- Stimuli relevant to Social Psychology					
Achievement	23	8	18	need	goal
Affect	A	13	14	emotion	effect
Anxiety	22	11	17	frustration	fear
Attitude	A	17	20	opinion prejudice component	good
Crowd	AA	8	14	mob	people
Fantasy	4	13	22	dream	dream fiction
Frustration	1	4	18	aggression	anxiety
Relativity		10	16	theory	Einstein
Role	11	12	14	playing	part people play
Snow	AA	12	10	cold	white
Stereotype	1	15	20	prejudice	same
Survey	32	12	18	sample	course look
Class II -- Stimuli relevant to Electronic Circuit Design					
Augment	7	11	9	increase	add change
Complex	13	18	12	difficult oedipus	variable
Current	A	17	11	electric electricity new problem river water wave	voltage
Direct	AA	15	13	indirect	current
Dissipation	1	21	17	loss	loss
Hybrid	5	15	8	plant	parameter
Plate	A	17	14	spoon	current
Plot	36	16	20	plan	graph
Pole	A	6	7	north	zero
Real	AA	18	9	true	imaginary
Transient	5	16	11	fleeting	response
Zero	11	16	16	cold degrees	nothing

* Thorndike - Lorge Frequency count

Table 1 (continued)

Class III -- Stimuli judged ambiguous with respect to Social Psychology or Electronics

Bias	5	14	12	distortion	grid
Coding		16	8	problem	form
Control	AA	14	18	group	grid systems
Factor	35	19	18	analysis	number
Frequency	4	16	17	occurrence often distribution	response
Power	AA	18	17	authority	watts

SECTION III.B

ENGINEERING TEACHING PROGRAMS: THE NATURE OF THE RESPONSE

F.W. Phelps, Jr. collaborated in this problem. This includes a short experiment on FORTRAN arithmetic carried out under Grant No. 7-30-0410-192. The experiment is re-included here because its interpretation is clarified by the later experiments, concluded under the present grant, that also bear on this domain.

Programmed learning experiments have frequently concentrated upon response attributes: covert vs. overt, selected vs. constructed, confirmation-feedback-reinforcement. Although it is difficult to generalize across experiments because of different kinds of subject matter, different programming styles, or employment of very different kinds of subjects, the general tenor of results has been negative with few exceptions (Review of Education Research, 1961; Lumsdaine, 1961; Keislar and McNeil, 1962; Williams, 1963; Tobias and Weiner, 1963). Some exceptions to the general trend provoke curiosity, however. Overt response modes have sometimes led to increased learning with novel and technical items (Fry, 1960; Williams, 1963), with tasks where writing seemed to be more than an incidental component (Cummings and Goldstein, 1962), and with long programs (Holland, 1960). Also, delayed tests have occasionally revealed differences when immediate tests did not (Krumbolz and Weisman, 1962). These several exceptions prompted the series of experiments reported below.

The first experiment uses training material (FORTRAN arithmetic) that appears to be both technical and novel, and requires writing as an intrinsic part of the task. Both immediate and delayed tests for retention are included. The second experiment uses programmed course notes on operator graphs, a difficult and long program, and also includes delayed and immediate tests of retention. The third experiment was essentially a replication of the second, where again a long and difficult set of programmed notes in the field of systems engineering constituted the topic of instruction. All three experiments were conducted with engineering undergraduates enrolled in a course in linear systems and design at the Johns Hopkins University.

Experiment I.[1]

Method. Two booklets to teach FORTRAN arithmetic were prepared. These booklets were identical, except that one version required students to respond explicitly, i.e. write answers to examples before consulting correct answers. The other version required merely that students read examples and read answers. Exactly the same information was supplied in each booklet.

Beginning engineering students were divided into five ability strata on the basis of mathematical aptitude scores obtained from college records. Half of each stratum was randomly allocated to an experimental group (writing explicit answers), and half to a control group (reading equivalent material). Both groups worked through the material and spent an equivalent amount of time studying it (about 20 minutes). The non-writing group was specifically instructed to continue re-reading material if necessary until time was called. Immediately thereafter, a short test (16 items) was administered to both groups. Two days later, an unannounced test was given. This unannounced delayed test was equivalent but not

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Also reported in final Report - Title VII Project No. 1012.

[1] Copies of the experimental materials are available upon request.

identical to the immediate test, having the same kind and number of items.

Results. The numbers of errors on the two tests were subjected to an analysis of variance (Table 1). The performance of the two groups was almost identical, and students of various ability levels did not appear to be differentially affected by the two procedures.

The material used, FORTRAN arithmetic, was selected because digital programming is novel material and seems to depend upon writing of symbols and characters according to very specific rules. These rules, in some instances, run directly counter to long and well-established habits. Because of the expected proactive interference and the direct involvement of a motor response, it was hypothesized that practice in writing specific responses would lead to better performance than merely reading through examples. The hypothesis was infirmed. The increase for both groups from the first test to the second is irrelevant to the present purpose, but occurred irrespective of whether Ss studied programming between tests.

Experiment II

Method. An extensive linear programmed sequence on operator graphs was prepared as part of an engineering course in systems and design. This material includes questions with answers provided a page or two hence, out of direct view. A student reading the material comes upon a question, and may attempt to answer the question independently before consulting the answer provided.

The experiment was scheduled for a four-hour time period (on a Saturday) and students were paid to participate. Students were randomly divided into a control group and an experimental group, subject to the restriction that the two groups were equated for class performance up to

Table 1. Analysis of Variance, Experiment I, FORTRAN Arithmetic, Error Scores on Immediate and Delayed Tests

Source of variance	d.f.	MS	F
Between Individuals	79		
Experimental vs. Control	1	6.80	
Strata (ability)	4	8.64	1.72
EC X S	4	1.85	
Residual (error bet.)	70	5.02	
Within Individuals			
Test$_1$ vs. Test$_2$	1	9.50	4.87[a]
T_1T_2 X Strata	4	0	
T_1T_2 X EC	1	0	
T_1T_2 X EC X Strata	4	0.43	
Residual (error with.)	70	1.93	

[a] Significant beyond the 5% level.

the time of the experiment (total points scored in two previous hour examinations). Both groups were given the same 42 pages of programmed material on operator graphs. The experimental group was instructed to try hard to answer questions in the text before consulting the answers provided. They were given a fifteen page booklet of blank paper and urged to write extensively in their booklets. Later examination of these booklets suggests instructions were followed.

The control group was instructed not to attempt to formulate an answer to questions in the text before consulting the answer given. They had a sheet of scratch paper and were requested to write as little as possible. Both groups were allowed three hours for study, and remained in a large lecture hall with the experimenters for the entire time. After study materials were collected, a one hour test ensued.

Results. Scores on the hour test were subjected to an analysis of variance (Table 2). As expected Table 2 shows that past performance in the course is a significant source of variance. Table 2 also suggests that there is no difference between the experimental and control treatments and this finding agrees with the outcome of many similar shorter experiments cited earlier. The third line in Table 2, however, shows that the variance attributable to interaction between treatment and previous performance is significant at about the 5% level.

The nature of this interaction is apparent in Table 3, showing mean score for each treatment - performance sub-group. The mean scores for the two halves of the control group differ little (16.1 vs. 15.2 for high and low performance groups, respectively). There is a large difference,

Table 2. Analysis of Variance, Error Scores in Hour Test, Experiment II

Source of Variation	d.f.	MS	F
Experimental vs. Control Group	1	.68	
Performance (High vs. Low)	1	158.46	7.01[a]
Interaction (EC X P)	1	91.64	4.05[b]
Residual	40	22.62	

[a] *Significant beyond the 1% level.*

[b] Significant beyond the 5% level.

Table 3. Mean Score by Treatment-Performance Group, Experiment II

		Treatment Group	
		Exptl.	Control
Previous Performance	High	18.7	16.1
	Low	12.0	15.2

however, between the two halves of the experimental group. High performance students average 18.7 points on the test while low performance students average 12.0. For high-performance students, construction of an answer prior to writing the answer apparently aids learning. Just the opposite appears to be the case for low-performance students, who appear to learn more from reading the answer immediately after reading the question.

The results of this experiment are probably of practical significance, because the differences produced approach the magnitude of differences associated with past performance. Results confirm previous research since they show no overall difference between response modes. The confirmation of previous results is subject to important qualification: students' competence in the subject matter.

The groups were re-tested again ten days later. It was impossible, of course, to control the activities of the two groups over the intervening time, but there was no difference between the two groups on re-test. Since making parallel and equivalent tests for this kind of material is very difficult, the conclusion to draw is probably that the retention hypothesis was inadequately tested.

Experiment III.

Method. An attempt was made to replicate Experiment II. Again students were divided into "high" and "low" strata on the basis of previous hour examinations, and randomly assigned to experimental and control groups. Again, extensive programmed materials on linear systems were used, and three hours devoted to their study. The experimental group, as in Experiment II, was instructed to try very hard to answer questions posed in the text before consulting answers, while the control group was requested to read answers directly after reading questions. Experiments II and III are identical except for study material.

Results. Errors scores were analyzed (see Table 4) and no significant treatment differences emerged at or beyond the 5% level. In particular, the interaction between ability (as measured by previous performance in the course) and response mode was not significant.

The treatment difference ($F_{1,44} = 2.76$), at about the 10% level was deviant enough to motivate a more careful scrutiny of the data. For students in the lower half of the ability distribution (those below the mean in performance in hour examinations preceding the experiment), merely reading answers led to fewer errors - 2.33 fewer errors on the average. A one-sided t-test for these students only is significant beyond the 5% level. That poorer students were hindered by attempts to compose responses is exactly what was observed as one part of the significant interaction in Experiment II. The complementary observation, that better students were helped, was not replicated, as the non-significant treatment-X-performance interaction in the present experiment attests.

Discussion

These experiments address the problem of response mode, especially in terms of exceptional findings previously reported that are puzzling. The strong interaction observed between response mode and ability in the second experiment was only partially replicated in the third. There was, of course, no interaction of this kind in the short experiment on FORTRAN arithmetic. The positive results occurred with long programs (over 40

Table 4. Analysis of Variance, Error Scores in Hour Test, Experiment III

Source of variation	d.f.	MS	F
Experimental vs. control group	1	28	2.76
Performance (High vs. Low)	1	93	9.18[a]
Interaction (EC X	1	8	----
Residual	44	10.13	

Beyond the 1% level.

typewritten pages of highly mathematical material), but other factors studied because of earlier suggestive findings, such as delayed vs. immediate retention tests and novel items, were not associated with positive results. Most experiments on response mode do not include ability level as a control variable, and of those we have seen, none reports an interaction. But the finding of no overall difference is completely compatible with the many previous null experiments that do not include ability level. If our ability groups are combined, there is no difference.

There seems to be a reasonable explanation for the interaction, moreover. Poorer students tend to benefit from immediate reading of the correct supplied answers because their attention is forced toward pertinent aspects of the subject. Put another way, a student who has not completely assimilated previous learnings may concentrate on trivial or irrelevant aspects of problems when he tries to construct answers. He thus wastes time on topics outside the realm of instruction. Students with a good understanding of previous material benefit from active attempts at problem-solving because they are getting direct practice on the kinds of items included in the criterion test.

These experiments do not resolve the ambiguities that motivated them. Rather they seem to suggest, at first thought, that still another variable - ability level - may be the key to reconciling previous diversities. In our opinion emphasis on ability per se is mistaken, and such emphasis will not lead to resolution of the exceptional findings that prompted the present set of experiments.

Instead of "ability", we feel the differential behavior linked with ability is the concept to command attention. The content of an earlier exceptional finding may unwittingly have produced responses of varying content that affected results. Thus the superior ability group performs better because it makes relevant responses. Or the less able group performs poorly because we, the experimenters, were not capable of providing sufficient cues to lead them to relevant responses. Relevance and cueing of responses are the aspects that cause significant changes in results. A similar point was made recently by Eigen and Margulies (1963), i.e., that overt responses are superior to covert only if a relevant response is called for and its information value is high. The preoccupation with response mode in programming studies to date perhaps has been unfortunate, because response mode may be one of the least significant components of learning behavior.

The foregoing leads directly to another matter. Many studies support the superior effectiveness of additional prompting compared with less prompting (Lumsdaine, 1961). (Implicitly it is often assumed by instructors that giving away the answer is undesirable, although maximum prompting is sound in terms of experimental findings.) One kind of maximum prompting is the kind used with the control group - reading a given answer immediately after reading a question. In order to use prompts other than actual presentation of the answers that would assure completely relevant responses, extensive empirical data are necessary. Incipient mistakes need to be corrected and skillful cueing must be provided if student responses are to be used effectively. Such data are almost never available. Therefore it seems likely that the value of the responses evoked, which must depend intimately upon the specific characteristics of the program, and of the learner, hold the key to how material is best presented. Without a careful standardization it may be preferable to avoid constructed responses.

A more general problem not raised by these experiments, as so far presented, is what variable should be measured. In all three experiments the criterion was performance on a written examination composed of items similar to, but not identical with, units in the programs. The restriction of interest to variables in the cognitive domain may prevent observation of outcomes that, for college students, are of greater import. Very recently Fiks (1964) reports that response mode affects attitudes toward programmed instruction when it does not affect performance. Affective and attitudinal variables linked to some of the less tangible products of learning, such as interest in professional literature, persistence of study without external pressure, etc., may over-shadow objective test results. A genuine attempt by students to answer questions, rather than a more or less passive exposure, may whet interest or encourage study habits conducive to independent research. This is a separate aspect of the response mode question.

A possible measure to use in programmed learning experiments is the frequency of question-asking by students as they study. If one method of study leads students to ask more questions than another, one group of students may acquire more knowledge than another. This enhanced knowledge would not necessarily be revealed, because an investigator constructs a test based on the materials handed out for study. If students are led to formulate and seek answers for many questions in addition to what is included in the study material, this additional learning cannot be revealed by the test. Rate-of-question-asking is a kind of variable that may be linked with higher-level kinds of learning, or with non-cognitive variables.

During the second experiment, students who asked questions of the experimenter were answered individually. (The students did not know of the experimenters' interest in the number of questions asked. Prior to the experiment, experimenters had agreed to give as little information as possible to students who asked questions so as to keep the information given constant for the two groups.) During the three-hour study period, sixteen students asked questions, and of these, fourteen were in the control group. Under the hypothesis that an equal number of questions will issue from the two treatment groups, this preponderance of questions from the control group is significant beyond the 1% level.

Various interpretations of this result seem equally tenable. If the experimenters had answered questions as asked, more learning might have resulted in the control group. A second possibility is that similar questions occurred to the experimental group, but were not vocalized, because this group with its technique of more rigorous study was able to answer its own questions. Still another explanation might be that the control group was less engrossed in the subject matter and used question-asking as a device to relieve boredom. If question-asking is used as an index of other significant aspects of learning, the control group is again favored over the experimental group.

All in all, these experiments suggest that long programs, of length realistic in terms of college courses, should probably not require students to construct answers unless there is extensive pretesting. They also suggest that response mode is not a variable that molds behavior significantly, that within a single mode are many variations in response (relevance of response) far outweighing mode itself in influencing behavior. Earlier findings of occasional differences associated with response mode may have stemmed from other factors unknowingly confounded with response mode.

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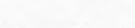
SECTION III.C. WORD ASSOCIATION RESPONSES TO VERBAL STIMULI VS. EQUIVALENT PICTORIAL STIMULI

It is commonly assumed that response hierarchies obtained from group of individuals also obtain for single individuals. Symbolism concerned with circuitry as a topic happens to offer one indirect experimental method for testing this assumption. Small pictorial symbols are used to represent circuit concepts when drawing circuit diagrams. These same symbols may be referred to by words. For instance the symbol "" stands for "resistor". Since there are many such symbols with parallel verbal representations, this offers a method for eliciting associations to equivalent stimuli on two different occasions by the same individuals. This might offer a method for testing whether an individual's response heirarchy resembles a hierarchy obtained from many individuals.

Method. Twenty-two Ss who were participants in a summer research group were given booklets containing small circuit symbols, like the resistance symbol depicted above. All had participated in conventional word association experiments earlier. They were instructed to give single words in response to small drawings, two for each drawing, on lines provided for that purpose immediately alongside the drawings. The symbols that were given both ways as stimuli are listed on the first column of Table 1.

In another section of the booklet equivalent verbal stimuli were given, and Ss were asked to write two different single word responses. The experimenter said the word aloud, waited 5 seconds for Ss to write a

Table 1. Responses for drawings and word; most popular response on two cycles.

	Responses to Drawings		Responses to Word	
Stimulus Presented	First	Second	First	Second
1. Ammeter Ammeter	Amplifier Amplifier	Flowgraph Operator	Current Current	Current Current
2. Capacitance	Capacitor	Capacitor Plates	Inductance Resistor	Capacitor
3. Cathode	Cathode	Tube	Plate Resistor	Resistor
4. Current Source	Current-Source	Current	Voltage-Source	Norton
5. Flowgraph	Flowgraph	Loop	Loop	Nodes
6. Flowgraph Loop	Loop	Feedback	Loop	Nodes
7. Grid	Grid	Tube	Plate	Cathode
8. Inductance	Inductor	Coil	Capacitance	Coil
9. L Circuit	Impedance	Voltage	Inductor	Inductor
10. Loop	Loop	Loop	Equation	Current Around
11. Matched Load	Variable	Load	Load	Impedance
12. Norton Source	Norton	Current	Thevenin	Current
13. Pi Circuit	Pi	T Circuit Impedance	T Circuit	Pi Delta
14. Plate	Plate	Tube	Cathode	Grid
15. Sine Wave	Sine	Wave	Wave	Cosine
16. Sinusoid	Feedback	Loop	Wave	Cosine
17. Source	Source	Current	Voltage	Current
18. Stray Capacitance	Stray	Capacitance	Tube	Inductance

Table 1 (continued)

	Responses to Drawings		Responses to Word	
Stimulus Presented	First	Second	First	Second
19. T Circuit	T Circuit	Pi	Pi	L Circuit
20. Thevenin Source	Thevenin	Voltage	Circuit	Impedance
21. Transformer	Transformer	Coils	Inductance	Coils
22. Transistor	Transistor	Emitter	Tube Vacuum Tube	Emitter
23. Triode Amplifier	Amplifier	Tube	Tube	Circuit
24. Tuned Amplifier	Amplifier	Amplifier	Frequency Tube	Resonance Voltage
25. Vacuum Tube	Tube	Triode	Voltmeter	Grid
26. Voltage Source Voltage Source	Voltage Voltage	Voltage Source	Current Current Current S	Current Current

response, and then said the word again, with a 5-second period for response. Since a reply to one form of stimulus might influence the reply to the parallel stimulus, the group was divided in half, with one half given pictures and then word stimuli, and the other half given the reverse.

Results. Tabulation of the first and second responses to both kinds of stimuli revealed that order of presentation was unimportant. There was no systematic difference between groups given first picture and then words vs. the reverse order. Results therefore are combined for further analysis.

Table 1 lists the most popular responses to drawings and to word stimuli. It is clear that the first response to a pictorial symbol is the word which was the parallel verbal stimulus. For instance, a small drawing of a cathode most often elicits the word "cathode" as a response. In all but four instances (stimuli 1, 9, 11, and 16) the first response to the drawing is a word that names the drawing. In other words, the primary response to a drawing is most often the stimulus in its verbal form. The exceptions involve possible ambiguities in interpreting the drawings that need not concern us further.

One might hope that if the two sets of stimuli are truly equivalent, that after the first, representational, response, the second response to a pictorial stimulus would be the same as the first response to a verbal stimulus. That is, if we grant the tendency to "name" a picture as an overwhelming first response to a pictorial symbol, it might be hoped that the secondary verbal association would match the primary association elicited by the verbal stimulus. Examination of Table 1 does not confirm this hope. The two kinds of stimuli match in the above way in only 6 out of 28 occasions.

Locking down contiguous columns of the table and comparing first and second responses to drawings and word, one can see that first and second responses to one kind of stimulus bear as much resemblance to one another as do the responses to different forms of the same stimulus.

It appears that these stimuli, although supposedly possessing equivalent meanings, activate rather different responses. In only six cases is the most popular second response to a drawing the same as the first response to a word. Although we do not have enough evidence to draw very firm conclusions, one gets the impression from inspecting the associates to the verbal stimuli that the characteristic type of associate is different for the two forms. There are syntagmatic associates to the verbal stimuli ("cathode" - "resistor"; "loop" - "equation";) and also quite a few contrast responses ("capacitance" - "inductance"; "current source" - "voltage-source"; "grid" - "plate"; "inductance" - "capacitance"; "Norton source" - Thevinen"). Because of the nature of circuits there are many contrast responses that happen to exist. These syntagmatic and contrast responses do not occur where stimuli are presented graphically, but these two tendencies are extremely important in explaining word associations generally. Particularly, contrast responses can account for large fractions of association data (see Entwisle, D., Form Class of Children's word associations, J. verb Learning verb. Behav. in press). The conclusion is that stimulation via one sensory avenue (auditory) appears to activate rather different response hierarchies than stimulation via another avenue (visual). This implies that the dual presentation of the stimuli did not lead to a test of the kind we hoped to develop. It did, however, happen to suggest the very interesting notion that a different response hierarchy may be activated by equivalent stimuli presented via two different sensory avenues. The auditory presentation apparently triggers verbal habits not tapped by the visual presentation.

For stimulus words where pictorial representations are not feasible, it has been assumed (cf. Deese, 1962)[1] that the initial response is a representational response, a covert repeating of the stimulus word by the subject. Although this assumption is difficult to verify directly, the evidence from our pictorial stimuli and their correspondence with word stimuli suggests that initial representational responses do occur.

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[1] Deese, J. The Associative Structure of Meaning, Psychol. Rev., 1962.

SECTION III.D

CONSTRICTION OF WORD ASSOCIATIONS CONCOMITANT WITH TRAINING

In the past decade the relation between language and cognition has frequently been viewed in terms of verbal mediation and dimensional salience. Classical word association techniques, when used to study these constructs, have offered some provocative findings. For example, response dominance is positively correlated with efficiency of concept manipulation (Romanow, 1958), and structured patterns of response characterize efficient problem solvers (Johnson, 1964). Thysell and Schulz' (1964) recent experiments with artificial verbal materials confirm that relevant associations increase concept fluency. More interestingly, they also show the converse, that strength of irrelevant associations reduces efficiency of concept utilization.

In an experiment on word associations for persons in different academic areas we saw that apparently training constricted the associative process. Engineering students gave many fewer different responses to engineering words than non-engineers. The assumption that this constriction paralleled training, or stemmed from training, could not be tested, however, because both groups were sampled at only one point in time.

By sampling associations of engineering students at the beginning of a training period and then again two months later, we can provide a more direct test of the constriction of associations concomitant with training.

Method. Twenty-two male engineering students, participating in a research study, were given the task of associating to 75 verbal stimuli on two occasions. The two occasions were separated by nine weeks' training in electronic circuits. Each stimulus was read aloud four times, with 5 seconds intervening between readings. Subjects were requested to write associations in special booklets and to try to give independent associations on each repetition. The instructions were:

"We would like you to give some word associations - single words in response to a stimulus word. The procedure will differ today, however, from the procedure used the other day. Today I will say aloud a number, then the stimulus word, and I would like you to write down the first word it makes you think of. I will then repeat the word, and I would like you to write another word association. I am going to repeat each stimulus word 4 times, and give you a few seconds each time to write an association. An example will show how the procedure goes:

Suppose this is your sheet: I will say "cat" "cat" "cat" "cat"

1. _____ _____ _____ _____

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any questions?

2. _____ _____ _____ _____

Results: Associations were tabulated, and the number of different responses tallied for the four repetitions on the two different administrations. If the number of associations is compared, repetitions being kept distinct, it is found for the first association given that the number of different associations is constricted. For second, third and fourth repetitions, results are less clear-cut, but by the fourth administration the directionality of change is equivocal (see Table 1). There are just as many increases as decreases.

Table 1. Comparison of Associations at Beginning and End of Training Number of Different Associations -- Administrations in June and July, compared

	Same	Greater	Less
First repetition	12	15	48
Second repetition	15	27	33
Third repetition	11	26	38
Fourth repetition	9	33	33

For the first association only, since this appears to be the association that is affected, the average number of different responses decreases from 11.2 in June to 9.9 in July. It must be kept in mind that these students had already had considerable exposure to most of the words on the list via a preceding course in linear systems. The large constriction in associations must occur with initial exposure - this is why we observe relatively large differences between the social psychology students and the engineering students in the ambiguous stimuli experiment reported earlier. But it is clear that training serves to limit the number of different associations.

The list of stimulus words used is given in Table 2. It was the same on both occasions.

Our results are relevant to other studies involving engineering

Table 2. List of Stimulus Words Presented on Two Occasions

1. Cathode
2. Source
3. Norton equivalent
4. Loop
5. Flowgraph
6. Voltmeter
7. Thevenin equivalent
8. Voltage source
9. Dissipation
10. Real
11. Current
12. Hybrid
13. Augment
14. Ammeter
15. Direct
16. Plot
17. Current Source
18. Power
19. Parameter
20. Half-power
21. Circuit
22. Two-Stage
23. Second-Order
24. Ploynomial
25. Configuration
26. Imaginary
27. Compensation
28. Decibels
29. Neper
30. Equalization
31. Logarithm
32. Bias
33. Positive
34. Control
35. Open
36. Quiescent
37. Anode
38. Alternation
39. Impedance
40. Negative
41. Capacitance
42. Angle
43. Amplitude
44. Coupling
45. Frequency
46. Factor
47. Phase
48. Characteristic
49. Zero
50. Transient
51. Exponential
52. Pole
53. Transfer function
54. Complex
55. Excitation
56. Plate
57. Vacuum Tube
58. Transformer
59. Sinusoid
60. Pi Circuit
61. Grid
62. Amplifier
63. Capacitance
64. L Circuit
65. Voltage
66. Transistor
67. Inductance
68. Triode
69. Stray Capacitance
70. Two Circuit
71. Energy
72. Matched
73. Triode Amplifier
74. Load
75. Tuned amplifier

personnel and also to experiments relating associations to learning. Saunders (1963) states that he followed up a notion that seems to be implicit in Guilford's originality factor, that the difference between a common and a rare response was important. He found that the number of common responses turned out to be the best single predictor of success, where job success was rated by supervisors. The subjects were engineers in large companies (Bell System, Detroit Edison, B. F. Goodrich, IBM, and Westinghouse) with five to seven years of work experience.

Substantially the same finding is reported by Hills (1958) who found that scores based on common responses were related to job placement and job success for experienced engineers. The task was to write as many synonyms as possible for eight common words.

Our work differs from the above because we are studying changes in associative patterns over time, but we find the pattern tighter after students have accummulated knowledge and experience.

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A Note on Consultants. A very striking piece of evidence concerning the overall competence of the students and their success in using the JOBSHOP simulation is afforded by the general experience we had with consultants. Early in July, 1964, we began systematic efforts to recruit consultants, and one of us (W. H. Huggins) personally contacted former students and others employed in local industries. By and large we were almost without success in getting useful results from persons employed in industry. Two exceptions were men employed by the Westinghouse Electric Corporation, Baltimore, and one of these men is enrolled in the E. E. Master's Degree program in the evening division of the University.

A meeting was held with a group of six men at the Bendix Corporation in Towson, Maryland. Initial enthusiasm did not lead to any attempts to solve the problem, in spite of the attraction of the consulting fee and the encouragement of supervisory personnel. A meeting was held with 14 men at the Westinghouse Electric plant. No one here did the second problem, and performance on the first problem was